UNIVERSITY OF CALIFORNIA AT BERKELEY
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EE105 Lab Experiments

Lab 6: Differential Amplifier Lab

Contents

1 Introduction

In certain applications, you only want to amplify the difference (which carries the useful information) of the two input signals but suppress the common part (most likely the noise) of them. Differential amplifier satisfies such requirement with its superior high differential signal gain over the common signal input. In the prelab, you already design a differential amplifier through hand analysis and simulation to satisfy various specs. In the lab, you will implement the design from the prelab and test its performance and adjust some design parameters if necessary

2 Materials

All the components you need in this lab are listed in Table 1.

Table 1: Lab 6 Components

Component	Quantity
CA3806	1
1nF	1
100uF	2

CA3806 provides five geneneral-purpose NPN transistors on a common monolithic substrate. So they are well-matched than those individual discrete NPN. The pinout diagram of CA3806 is shown as below:

Make sure the substrate(Terminal 13) is connected to the most negative voltage in your circuit. For more useful information, please refer to the datasheet.

3 Design Specs

The overall schematic is shown in Figure 2. The design specs is shown in Table 2. You will use Q1 and Q2 in CA3806 to implement the differential input stage and use Q3 and Q4 to implement the Widlar current mirro.
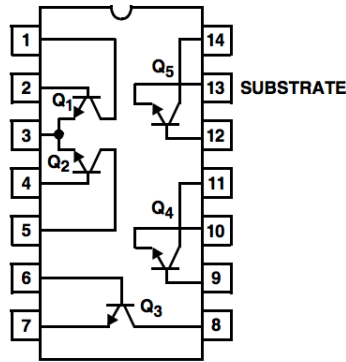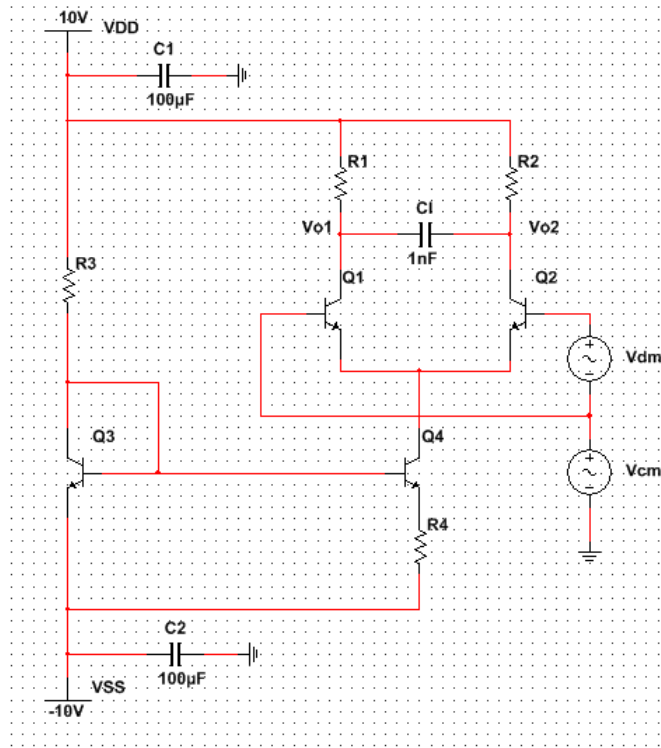
Figure 1: CA3809 Pinout

Figure 2: Overall Schematic

Table 2: Design Specification

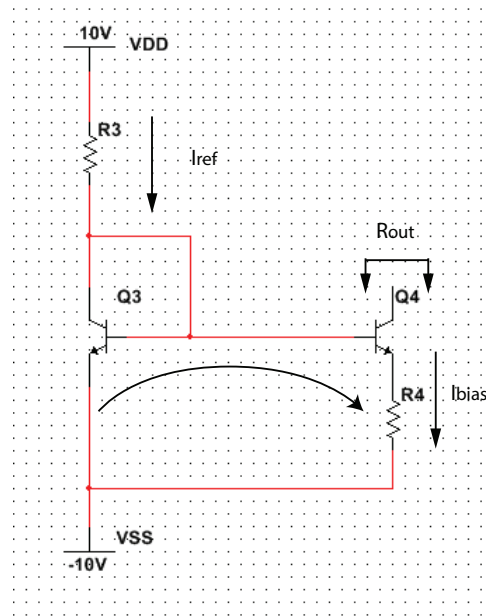|	
Differential Signal Gain $((V_{o1} - V_{o2})/V_{dm})$	$\geqslant 80$
Differential Signal High Cutoff Frequency $(f_{H_{dm}})$	$\geqslant 20\text{kHz}$
Differential Output Swing $(V_{o1} - V_{o2})$	$\geqslant 2\text{V}$ (peak to peak)
Supply Voltage (V_{DD}/V_{SS})	10V/-10V

4   Widlar Current Source

Figure 3: Widlar Current Mirror

Implement the current mirror as shown in Figure 3. Measure I_{ref}, I_{bias} and R_{out}. When you measure I_{bias}, you can connect the collect of Q4 thought a resistor to VDD and make sure that the collector voltage of Q4 is above -2V. To measure R_{out}, you can connect the collector of Q4 through two different resistors to VDD and make sure that the collector voltage of Q4 is always above -2V. Record the collector voltage and collector currents under those two cases. Then R_{out} can be determined from the ratio of the voltage difference verse current difference.
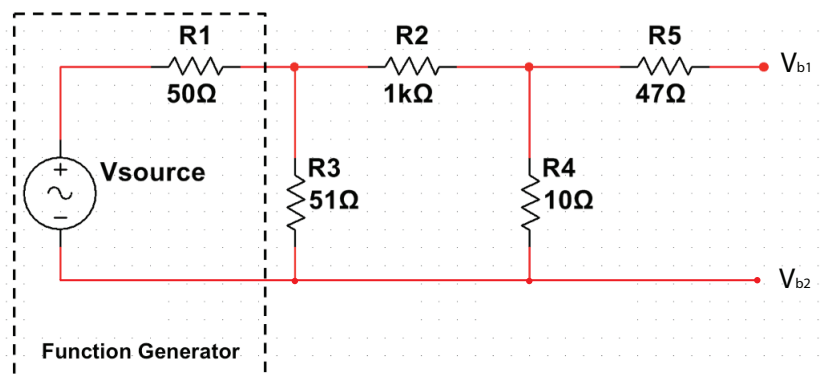
5   Differential Mode Characterization

Figure 4: Input Attenuation Network

After you adjust the current mirror properly. You can connect the current mirror with the differential pair. To measure the differential gain, you will need the attenuation network that you used in the previous

lab. You must be careful for setting the base voltage of differential pair. In the prelab, you already work out a suitable range for the base voltage. Use the mean of that range to bias both Q1 and Q2's base so that you can maximize the input range. The way to set it up is to connect the base of either Q1 or Q2 to a DC supply with the voltage as the mean of the allowable base voltage range. Then connect function generator through the attenuation network in the way as shown in Figure 4 and set the offset voltage of the function generator to be the same voltage. The magnitude of the function generator should be selected so that the maximum and minimum base voltage do not exceed that range after attenuation network.

To measure the differential output voltage, you need the difference of V_{o1} and V_{o2}. To do that, you will use the math function of the oscilloscope. If you don't know how to use that, please ask the GSI for help. Check if the gain, bandwidth and output swing satisfy the design specs and tune design parameter if necessary.

Save the traces showing both differential input and differential output at a frequency below the cutoff frequency. Record the differential signal gain from 100Hz to 100kHz with 10 points per decade. Plot the Bode plot with data you record. Mark the differential signal gain A_{dm} and cutoff frequency $f_{H_{dm}}$ on the curve.

6   Common Mode Characterization

Next you will characterize the common signal gain of the differential amplifier. Since the common signal gain is usually very small, you will not need the attenuation network. You can directly short the base of Q1 and Q2 together and apply a sine wave with proper magnitude and offset voltage. The offset voltage is again set to the mean of the allowable input range. The magnitude is selected so that the maximum and minimum voltage on the base do not exceed the range but large enough to make output observable.

Save the traces showing both the common input and differential output at a frequency below the cutoff frequency. Record the common signal gain from 100Hz to 100kHz with 10 points per decade. Plot the Bode plot with data you record. Mark the common signal gain A_{cm} on the curve and explain why the the frequency of the common mode gain is different from that of the differential mode gain if there is any.

Measure the load resistor values and check the measured common mode gain against the simulation.