Circuit Symbol for NMOS

4 terminal including Body (Arrow pointing to channel indicating substrate is p-type)

Modified circuit symbol with arrow on source (Arrow indicating direction of current flow)

Simplified circuit symbol with body connected to source (or when the effect of the body on device operation is unimportant)

Note in NMOS
1. Drain voltage is always more positive than Source voltage
2. Current always flows from Drain to Source
I-V Curves of NMOS

\[ i_D = \frac{1}{2} k_n (\frac{W}{L}) V_{OV1}^2 \]

\[ v_{DS} \leq v_{OV} \] Triode region

\[ v_{DS} \geq v_{OV} \] Saturation region

\[ v_{DS} = V_{sa} + V_{OV4} \]

\[ V_m \text{ is threshold voltage of NMOS} \]

Relative Voltage Levels of NMOS

Analog circuit (e.g., linear amplifiers) usually biased in Saturation region

Digital circuit (e.g., inverter) use Triode region as one of the states

\[ V_m \text{ is usually fixed once a process (technology) is selected} \]
Drain Current vs Gate Voltage

In Saturation Region
\[ i_D = \frac{1}{2} \mu_m C_{ox} \frac{W}{L} V_{GS}^2 \]
\[ = \frac{1}{2} \mu_m C_{ox} \frac{W}{L} (V_{GS} - V_m)^2 \]

To experimentally determine \( V_m \):
Measure and plot \( \sqrt{i_D} \) versus \( V_{GS} \)
\[ \sqrt{i_D} = \frac{1}{2} \mu_m C_{ox} \frac{W}{L} (V_{GS} - V_m) \]
\( V_m \) = intercept with horizontal axis

Finite Output Resistance due to Channel Length Modulation

When \( V_{DS} = V_{GS} \), the channel pinch of near the Drain. With further increase in \( V_{DS} \), the pinch off point moves slowly towards the source, effectively reducing the channel length from \( L \) to \( L - \Delta L \) (this is called "channel length modulation"):

\[ i_D = \frac{1}{2} \mu_m C_{ox} \frac{W}{L - \Delta L} (V_{GS} - V_m)^2 \]

The continual increase of \( i_D \) with \( V_{DS} \) is modeled by
\[ i_D = \frac{1}{2} \mu_m C_{ox} \frac{W}{L} (V_{GS} - V_m)^2 (1 + \lambda v_{DS}) \]
Output Resistance of MOSFET

\[ i_D = \frac{1}{2} \mu C_m W L (V_{GS} - V_t)^2 (1 + \lambda V_{DS}) \]

\[ r_o = \left( \frac{\partial V_{DS}}{\partial i_D} \right)_{V_{GS}=V_{DS}} = \left( \frac{\partial i_D}{\partial V_{DS}} \right)_{V_{GS}=V_{DS}} = \frac{1}{\lambda} \left( \frac{1}{2} \mu C_m W L (V_{GS} - V_t)^2 \right) = \frac{1}{\lambda I_D} \]

\[ r_o = \frac{1}{\lambda I_D} \]

where \( I_D = \frac{1}{2} \mu C_m W L (V_{GS} - V_t)^2 \) is the DC bias current at Drain.

Circuit Symbol of PMOS

4 terminal including Body
(Arrow pointing away from channel indicating substrate is n-type)

Modified circuit symbol with arrow on source
(Arrow indicating direction of current flow)

Simplified circuit symbol with body connected to source (or when the effect of the body on device operation is unimportant)

Note in PMOS
1. Source voltage is always more positive than Drain voltage
2. Current always flows from Source to Drain
3. Source is usually drawn on top so current flows downward (convention)
PMOS I-V Equations

Triode Region:
\[ i_D = \mu C_{ox}\frac{W}{L}\left|v_{ds}\right|\left(v_{gs} - \frac{1}{2}v_{ds}^2\right) \]
\[ v_{ov} = \left|v_{gs}\right| - \left|v_t\right| \]
Use same equation as NMOS but add absolute sign on all voltages since most voltages are negative:
\( v_t < 0, \ v_{ds} < 0, \ v_{gs} < 0 \)
So either use \( v_{ds} \) or \( |v_{gs}| \)

Saturation Region:
\[ i_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left|v_{gs}\right|\left|v_{ov}\right| \]
\[ v_{gs} = \left|v_t\right| + \left|v_{ov}\right| \]
\[ v_{ds} < |V_t| \]

Relative Voltage Levels of PMOS

Digital circuit (e.g., inverter) use Triode region as one of the states
Analog circuit (e.g., linear amplifiers) usually biased in Saturation region

\( V_t \): threshold voltage of PMOS
\( V_t \) is usually fixed once a process (technology) is selected
Diode-Connected Transistor

With Gate connected to Drain, it becomes a 2-terminal device. This is called "diode-connected transistor". In this configuration, the transistor is always in "Saturaiton". Its I-V relationship is:

\[ i = I_D = \frac{1}{2} \mu_m C_m \frac{W}{L} v_{ov}^2 \]

\[ v_{gs} = v_{ds} = v \]

\[ v_{ov} = v_{gs} - V_m = v - V_m \]

\[ i = \frac{1}{2} \mu_m C_m \frac{W}{L} (v - V_m)^2 \]

Example Circuit (1)

Design Problem:
Determine \( R_s \) and \( R_D \) such that the NMOS is biased at \( I_D = 0.4 \) mA and \( V_D = 0.5 \) V. The NMOS has \( V_t = 0.7 \) V, \( \mu_m C_m = 100 \mu A / V^2 \), \( L = 1 \mu m \) and \( W = 32 \mu m \).

Solution:

\[ R_D = \frac{V_D - V_g}{I_D} = \frac{2.5 - 0.5}{0.4} = 5 \Omega \]

\[ I_D = \frac{1}{2} \mu_m C_m \frac{W}{L} v_{ov} = 0.4 \text{mA} \rightarrow v_{ov} = 0.5 \text{V} \]

(channel length modulation can usually be ignored when solving DC bias)

\[ v_{gs} = V_t + v_{ov} = 0.7 + 0.5 = 1.2 \text{V} \]

\[ V_G = 0 \text{ (grounded)} \rightarrow V_i = -1.2 \text{V} \]

\[ R_D = \frac{V_i - V_{gs}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 3.25 \Omega \]
Example Circuit (2)

The resistor divider is a common bias circuit.
To solve the DC bias condition, it means to solve
\[ I_D \cdot V_{GS}, V_{GS} \]

The NMOS has \( V_m = 1V \), \( k_a = \mu a C_m \frac{W}{L} = 1mA/V^2 \)

First, solve \( V_G = V_{DD} \frac{R_{G2}}{R_{G1} + R_{G2}} = 10 \frac{5}{5 + 5} = 5V \)
\[ V_{GS} = 5 - I_D R_S = 5 - 6I_D \] (with \( I_D \) in mA)

Next, assume the transistor is in saturation:
\[ I_D = \frac{1}{2} k_a V_{GS}^2 = 0.5(V_{GS} - V_m)^2 = 0.5(5 - 6I_D - 1)^2 \]
\[ 18I_D^2 - 25I_D + 8 = 0 \quad \rightarrow \quad I_D = 0.89mA \text{ or } 0.5mA \]
If \( I_D = 0.89mA \), \( V_{GS} = -0.34V \), NMOS will be cut-off
\( \rightarrow \) not a physical solution.
If \( I_D = 0.5mA \), \( V_{GS} = 2V \), \( V_{OV} = 2 - 1 = 1V \)
\[ V_{DS} = V_{DD} - I_D(R_D + R_S) = 10 - 6 = 4V > V_{OV} \]
Saturation assumption verified!

Example Circuit (3)

Design Problem:
Design the circuit such that \( I_D = 0.5mA \) and \( V_D = 3V \).
PMOS has \( V_p = -1V \), \( \mu, C_m(W/L) = 1mA/V^2 \).
Also find the maximum \( R_D \) for PMOS to remain in Saturation

Solution:
\[ I_D = \frac{1}{2} k_a V_{Gp} = 0.5mA \quad \rightarrow \quad |V_{Gp}| = 1V \]
\[ |V_{DD}| = |V_D| + |V_{GS}| = 1+1 = 2V \]
\[ V_s = 5V \quad \rightarrow \quad V_D = 3V \]
We can choose \( R_{G1} = 2M\Omega \) and \( R_{G2} = 3M\Omega \)
Saturation: \( V_D \leq 5 - |V_{GS}| = 4V \)
\[ R_{D, max} = \frac{V_{DD}}{I_D} = \frac{4}{0.5} = 8k\Omega \]