# EE105 – Fall 2015
# Microelectronic Devices and Circuits

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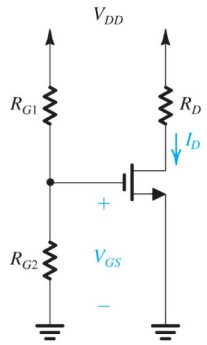
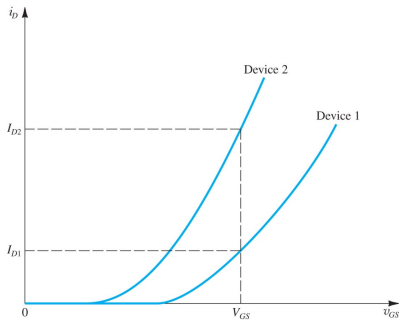
## Purposes of Bias Circuit

- Provide a stable bias drain (collector) current
- Bias insensitive to variations in
  - Transistor parameters (β for BJT, $V_t$, $k_n$ for MOS),
  - Temperature and other environmental changes
- Keep transistors in flat part of the I-V curves (Saturation for MOS, Active for BJT) for desired output swing



# Example of Non-Ideal Bias

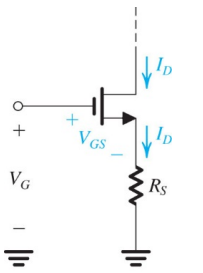


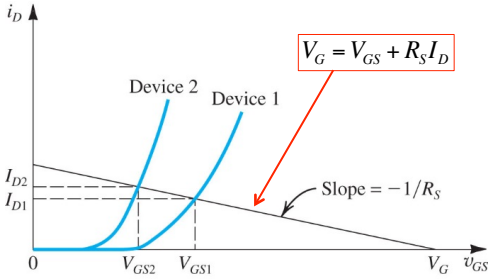




- Fixed $v_{GS}$ from voltage divider
- Large variation in $i_D$ due to device variations
- Large temperature dependence
  - $\mu_n$ and $V_t$ are temperature sensitive



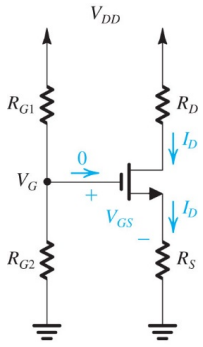
# Adding Source Resistance $R_S$



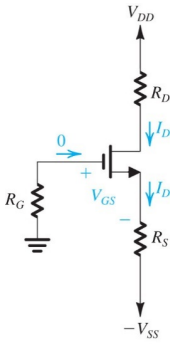




- $R_S$ provides negative feedback
  - If $I_D$ increases, $V_{GS}$ decreases → reduce $I_D$
  - If $I_D$ decreases, $V_{GS}$ increases → increase $I_D$
- Stabilize $I_D$ w.r.t. device and temperature variations

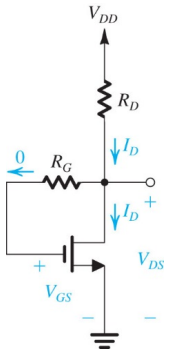
# Practical Implementations




Single Power Supply




Dual Power Supplies

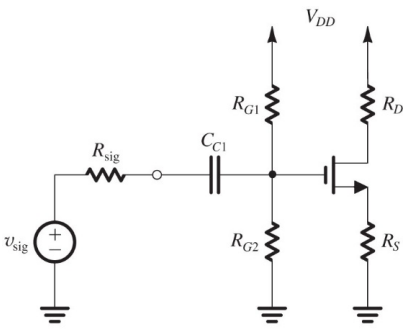



Drain-to-Gate Feedback





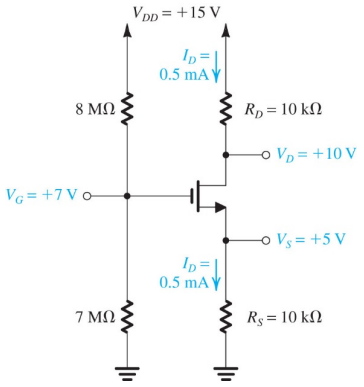
# Coupling Capacitor to Separate AC Signal from DC Bias




- Coupling capacitor is DC -open and AC-short
- Prevent signal source to change bias condition
- The coupling capacitor creates a lower bound of operating frequency

# Bias Design Example

**Goal: design bias for $I_D$ = 0.5 mA. MOS has $V_t$ = 1V and $k_n$ = 1 mA/V²**




General rule of thumb:

Equal (1/3 each) voltage drop across $R_D$, $R_S$, and $V_{DS}$

Choose $R_D = \dfrac{15\text{V} - 10\text{V}}{0.5\text{ mA}} = 10\text{ k}\Omega$

Choose $R_S = \dfrac{5\text{V} - 0\text{V}}{0.5\text{ mA}} = 10\text{ k}\Omega$

Determine $V_{GS}$ :

$0.5\text{ mA} = \dfrac{1}{2}k_n(V_{GS} - 1)^2 \Rightarrow V_{GS} = 2\text{V}$

$V_G = V_{GS} + 5\text{V} = 7\text{V}$

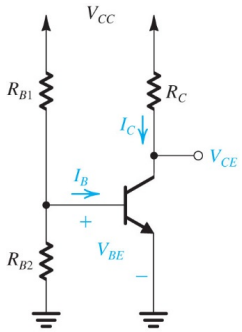
We can choose any combination of voltage divider, $R_{G1}$ and $R_{G1}$, that gives $V_G = 7$V.

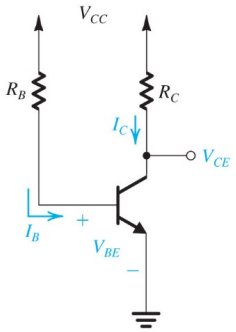
Remember $R_{G1} \parallel R_{G1}$ becomes $R_{in}$

So use large $R_{G1}$ and $R_{G1}$, in the MΩ range.



# Non-Ideal Biasing Schemes for BJT



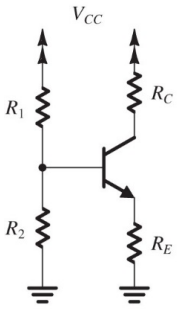



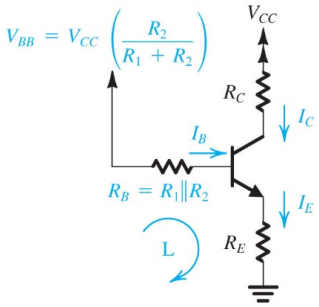

Since $i_C = I_S e^{\frac{v_{BE}}{V_T}}$ depends exponentially on $v_{BE}$, small variation in $v_{BE}$ leads to large change in $I_C$

$I_C = \beta\left(\dfrac{V_{CC} - 0.7}{R_B}\right)$

is sensitive to variation in $\beta$

# Good (Stable) Bias Circuits for BJT




Similar to MOSFET bias, but must consider finite base current:
First, find Thevenin equivalent circuit of bias circuit:

$$V_{BB} = V_{CC}\left(\frac{R_2}{R_1 + R_2}\right)$$

$$R_B = R_1 \| R_2$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{\beta + 1}}$$

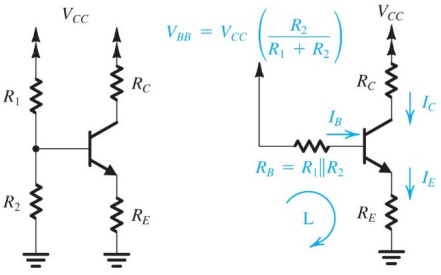
Choose $V_{BB} >> V_{BE}$ and $R_E >> \frac{R_B}{\beta + 1}$

$I_E$ is insensitive to variation in $\beta$ and $V_{BE}$



# Design Example of BJT Bias

**Goal: design bias circuit for $I_E$ = 1 mA with $V_{CC}$ = 12 V and β = 100**




General rule of thumb:

Choose $V_{BB} = \frac{1}{3}V_{CC} = \frac{12}{3} = 4$ V

$$V_E \approx V_{BB} - 0.7 = 3.3 \text{ V} \Rightarrow R_E = \frac{V_E}{1 \text{ mA}} = 3.3 \text{ k}\Omega$$

Choose $V_C = \frac{2}{3}V_{CC} = 8$ V, $R_C = \frac{12 - 8}{1 \text{ mA}} = 4$ kΩ

Choose bias current through $R_1, R_2$ to be $10I_B$

$$R_1 + R_2 = \frac{12}{0.1 \text{ mA}} = 120 \text{ k}\Omega$$

$$R_1 = 2R_2 \Rightarrow R_1 = 80 \text{ k}\Omega, R_2 = 40 \text{ k}\Omega$$

Check resulting $I_E$:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{\beta + 1}} = \frac{4 - 0.7}{3.3 + \frac{40 \| 80}{101}} = 0.93 \text{mA}$$

Adjust $R_E$: $I_E = 1$ mA when $R_E = 3$ kΩ