Why Differential?

- Differential circuits are much less sensitive to noises and interferences
- Differential configuration enables us to bias amplifiers and connect multiple stages without using coupling or bypass capacitors
- Differential amplifiers are widely used in IC’s
  - Excellent matching of transistors, which is critical for differential circuits
  - Differential circuits require more transistors → not an issue for IC
MOS Differential-Pair

Basic Configuration

Two matched MOS transistors
Common current bias
"Differential signals" applied to \(v_{g1}\) and \(v_{g2}\)
(equal amplitude but opposite sign)
"Differential outputs" are produced
at \(v_{d1}\) and \(v_{d2}\)

Note in differential configuration,
\(V_{g3}\) is fixed for both \(Q_1\) and \(Q_2\)
\(I_{d1} = I_{d2} = \frac{I}{2}\)
\(I = \frac{k_e}{2} (V_{g3} - V_w)\)
\(V_{g3} = V_w + \frac{I}{n k_e}\)

MOS Differential-Pair

Rejects Common-Mode Inputs

The common voltages applied
to both \(Q_1\) and \(Q_2\) are referred to as
common mode, \(V_{CM}\).
Common mode inputs usually come
from noises or interferences.
Differential pair should reject \(V_{CM}\):

Since \(V_{g3} = V_{g3} = V_w + \frac{I}{n k_e}\)
is fixed in differential pair,
\(V_{CM}\) simply changes the voltage at Source, \(V_S\).
The drain currents remain fixed:
\(I_1 = I_2 = \frac{I}{2}\)
\(v_{d1} = V_{dd} - \frac{I}{2} R_D = v_{d2}\)
Differential output \(v_{d1} - v_{d2} = 0\)
**Example**

$V_{DS} = V_{GS} = 1.5V, I = 0.4mA, R_s = 2.5k\Omega$. Minimum voltage across current source $V_{DS} = 0.4V$.

For $Q_1$, and $Q_2$: $k_s = 4mA/V^2, V_{in} = 0.5V$. Find $V_{in}, I_{Q1}, I_{Q2}, V_{G1}, V_{G2}$ for 3 different $V_{CM}$ below:

Due to symmetry, $I_{Q1} = I_{Q2} = I/2$ for all 3 $V_{CM}$ values.

- $V_{CM} = V_{G1} = 0.5V + 0.32V = 0.82V$
- $V_{in} = V_{G2} = 0.5V - 0.5I/2R_s = 1.5V - 0.2 \times 2.5V = 1V$
- Differential output $V_{in} - V_{G2} = 0$

Maximum $V_{CM}$ should keep $Q_1$ and $Q_2$ in saturation:

- $V_{CM} > V_{G1} - V_{in}$: $V_{G1} - V_{in} > V_{G2} - V_{in}$: $V_{CM} = V_{G1} = V_{in} + V_s = 1.5V$
- Minimum $V_{CM}$ should keep $V_{in}$ above minimum current source voltage, $V_{CT}$:

$V_{CM} = -V_{CT} + V_{CM} + V_{GS} = -1.5 + 0.82 + 0.4 = -0.28V$

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**Operation with Differential Input Voltage**

$$i_{Q1} = \frac{k_s}{2}(V_{GS1} - V_c)^2; \quad i_{Q2} = \frac{k_s}{2}(V_{GS2} - V_c)^2$$

$$\sqrt{i_{Q1} - i_{Q2}} = \frac{k_s}{2}(V_{GS1} - V_{GS2}) = \frac{k_s}{2}(V_{in})$$

Square both sides, and recall $i_{Q1} + i_{Q2} = I$

$$2\sqrt{i_{Q1} - i_{Q2}} = I = \frac{k_s}{2}(V_{in})$$

Substitute $i_{Q2} = I - i_{Q1}$, solve quadratic equation:

$$i_{Q2} = \frac{I}{2} \pm \sqrt{\frac{I}{2} \left( \frac{V_{in}}{2} \right)^2 - \frac{I}{k_s} \left( \left( \frac{V_{in}}{2} \right)^2 - \frac{I}{V_{in}} \right)}$$

$$\frac{I}{2} = \frac{1}{2} k_s V_{in}^2 \quad \Rightarrow k_s = I/V_{in}^2$$

$$i_{Q2} = \frac{I}{2} \pm \sqrt{\frac{I}{2} \left( \frac{V_{in}}{2} \right)^2 - \frac{I}{V_{in}} \left( \left( \frac{V_{in}}{2} \right)^2 - \frac{I}{V_{in}} \right)}$$
Operation with Differential Input Voltage

\[ i_{D1,2} = \frac{I}{2} \pm \frac{I}{V_{OV}} \frac{v_{id}}{2} \sqrt{1 - \frac{(v_{id}/2)^2}{V_{OV}^2}} \]

Near \( v_{id} = 0 \):

\[ \sqrt{1 - \frac{(v_{id}/2)^2}{V_{OV}^2}} = 1 \] (neglect high-order terms)

\[ i_{D1} = \frac{I}{2} + \frac{I}{V_{OV}} \frac{v_{id}}{2} \]

\[ i_{D2} = \frac{I}{2} - \frac{I}{V_{OV}} \frac{v_{id}}{2} \]

Current of Differential Pair for Various Overdrive Voltage

\[ i_{D1,2} = \frac{I}{2} \pm \frac{I}{V_{OV}} \frac{v_{id}}{2} \sqrt{1 - \frac{(v_{id}/2)^2}{V_{OV}^2}} \]

The linear range of operation of the MOS differential pair can be extended by operating the transistor at a higher value of \( V_{OV} \)
Small Signal Operation

For differential AC small signal, the differential pair is "anti-symmetric". The potential at the mid point (Source) is zero. This is called "Virtual Ground"

Differential mode voltage gain:

\[ A_d = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D \]

This virtual ground is obtained without using a large bypass capacitor ➞ much smaller area and better frequency response

Differential Half Circuit

Because the two halves of the circuits are anti-symmetric, and Source is at virtual ground, we can simplified and just analyze the "half circuit"

\[ Q_i \text{ biased at } \frac{I}{2} \]

\[ A_d = \frac{v_{o1}}{v_{id}} = g_m \left( R_D || r_s \right) \]
Differential Amplifier with Current-Source Loads

\[ Q_3 \text{ and } Q_4 \text{ are PMOS current sources (active loads)} \]

From half-circuit

\[ A_d = \frac{V_{os}}{V_{sd}} = g_{m1} \left( R_{o1} \parallel R_{o3} \right) \]

Cascode Differential Amplifier

Cascode configurations for both amplifying transistors and current source loads.

From half-circuit

\[ A_d = \frac{V_{os}}{V_{sd}} = g_{m1} \left( R_{o1} \parallel R_{op} \right) \]

\[ R_{in} = \left( g_{m1} R_{o1} \right) R_{o3} \]

\[ R_{op} = \left( g_{m2} R_{o2} \right) R_{o3} \]

If all transistors are identical,

\[ R_{in} = R_{op} = g_{m}^2 R_{o}^2 \]

\[ A_d = \frac{1}{2} g_{m}^2 R_{o}^2 \]