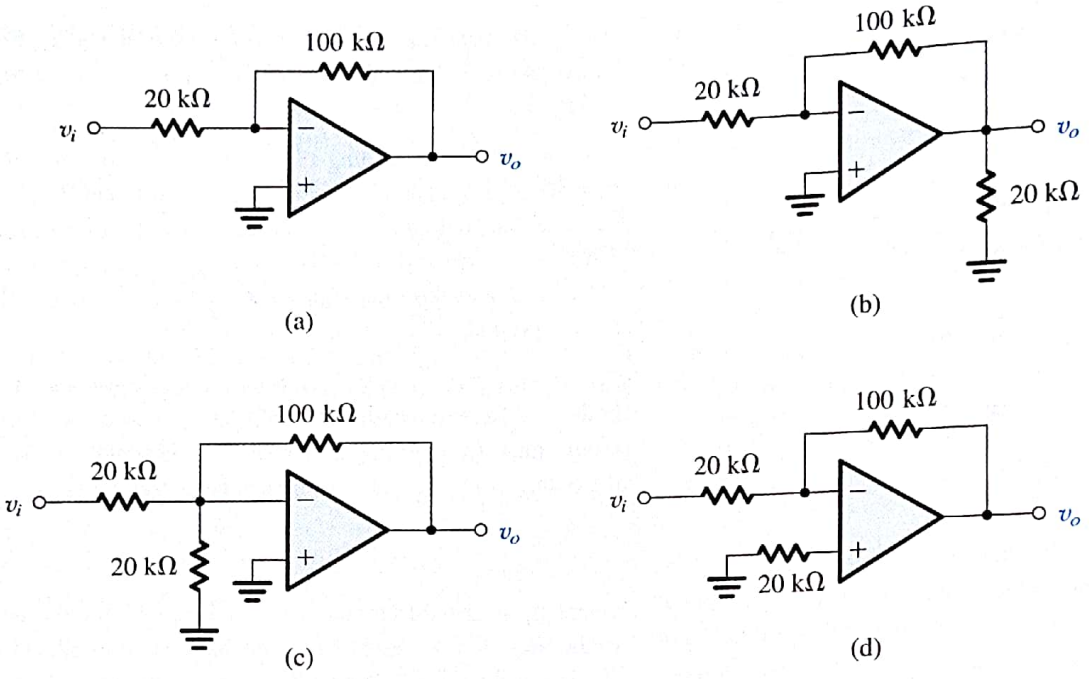


**Figure P2.8**

**2.10** You are provided with an ideal op amp and three 10-kΩ resistors. Using series and parallel resistor combinations, how many different inverting-amplifier circuit topologies are possible? What is the largest (noninfinite) available voltage gain magnitude? What is the smallest (nonzero) available gain magnitude? What are the input resistances in these two cases?

**SIM 2.11** For ideal op amps operating with the following feedback networks in the inverting configuration, what closed-loop gain results?

(a) $R_1 = 10\ \text{k}\Omega, R_2 = 10\ \text{k}\Omega$
(b) $R_1 = 10\ \text{k}\Omega, R_2 = 100\ \text{k}\Omega$
(c) $R_1 = 10\ \text{k}\Omega, R_2 = 1\ \text{k}\Omega$
(d) $R_1 = 100\ \text{k}\Omega, R_2 = 10\ \text{M}\Omega$
(e) $R_1 = 100\ \text{k}\Omega, R_2 = 1\ \text{M}\Omega$

**D 2.12** Given an ideal op amp, what are the values of the resistors $R_1$ and $R_2$ to be used to design amplifiers with the closed-loop gains listed below? In your designs, use at least one 10-kΩ resistor and another equal or larger resistor.

(a) −1 V/V
(b) −2 V/V
(c) −5 V/V
(d) −100 V/V

**D 2.13** Design an inverting op-amp circuit for which the gain is −10 V/V and the total resistance used is 110 kΩ.

**D 2.14** Using the circuit of Fig. 2.5 and assuming an ideal op amp, design an inverting amplifier with a gain of 46 dB having the largest possible input resistance under the constraint of having to use resistors no larger than 1 MΩ. What is the input resistance of your design?

**2.15** An ideal op amp is connected as shown in Fig. 2.5 with $R_1 = 10\ \text{k}\Omega$ and $R_2 = 100\ \text{k}\Omega$. A symmetrical square-wave signal with levels of 0 V and −1 V is applied at the input. Sketch and clearly label the waveform of the resulting output voltage. What is its average value? What is its highest value? What is its lowest value?

**2.16** For the circuit in Fig. P2.16, assuming an ideal op amp, find the currents through all branches and the voltages at all nodes. Since the current supplied by the op amp is greater than the current drawn from the input signal source, where does the additional current come from?

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to 40 dB. What is its value? What is the associated lower 3-dB frequency? Sketch and label the output that results with a 10-μs, 1-V positive-input pulse (initially at 0 V) with (a) no dc stabilization (but with the output initially at 0 V) and (b) the feedback resistor connected.

***2.84** A Miller integrator whose input and output voltages are initially zero and whose time constant is 1 ms is driven by the signal shown in Fig. P2.84. Sketch and label the output waveform that results. Indicate what happens if the input levels are ±2 V, with the time constant the same (1 ms) and with the time constant raised to 2 ms.

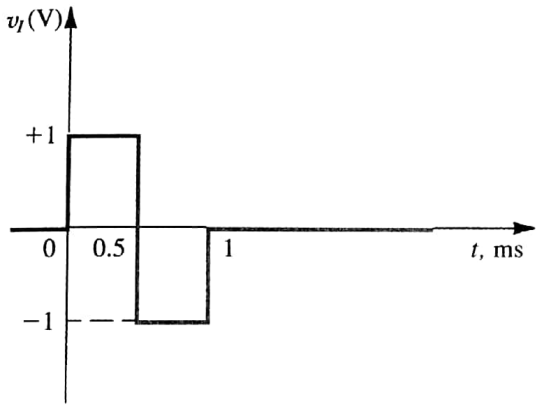


Figure P2.84

**2.85** Consider a Miller integrator having a time constant of 1 ms and an output that is initially zero, when fed with a string of pulses of 10-μs duration and 1-V amplitude rising from 0 V (see Fig. P2.85). Sketch and label the output waveform resulting. How many pulses are required for an output voltage change of 1 V?

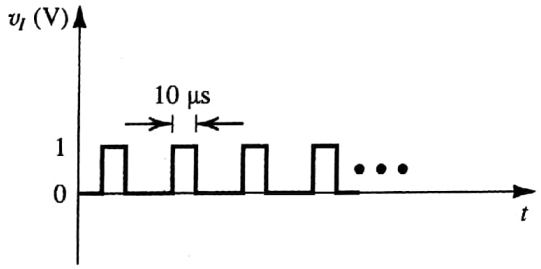


Figure P2.85

**D 2.86** Figure P2.86 shows a circuit that performs a low-pass STC function. Such a circuit is known as a first-order, low-pass active filter. Derive the transfer function and show that the dc gain is $(-R_2/R_1)$ and the 3-dB frequency $\omega_0 = 1/CR_2$. Design the circuit to obtain an input resistance of 10 kΩ, a dc gain of 40 dB, and a 3-dB frequency of 1 kHz. At what frequency does the magnitude of the transfer function reduce to unity?

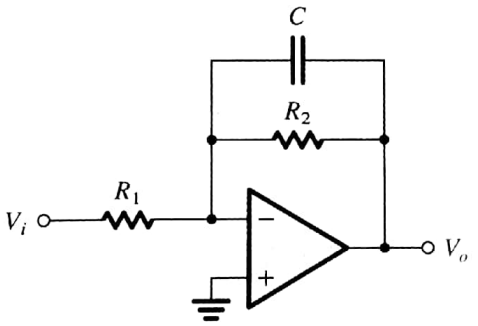


Figure P2.86

*2.87 Show that a Miller integrator implemented with an op amp with open-loop gain $A_0$ has a low-pass STC transfer function. What is the pole frequency of the STC function? How does this compare with the pole frequency of the ideal integrator? If an ideal Miller integrator is fed with a −1-V pulse signal with a width $T = CR$, what will the output voltage be at $t = T$? Assume that at $t = 0, v_O = 0$. Repeat for an integrator with an op amp having $A_0 = 1000$.

2.88 A differentiator utilizes an ideal op amp, a 10-kΩ resistor, and a 1-nF capacitor. What is the frequency $f_0$ (in Hz) at which its input and output sine-wave signals have equal magnitude? What is the output signal for a 1-V peak-to-peak sine-wave input with frequency equal to $10f_0$?

**2.89** An op-amp differentiator with 1-ms time constant is driven by the rate-controlled step shown in Fig. P2.89. Assuming $v_O$ to be zero initially, sketch and label its waveform.

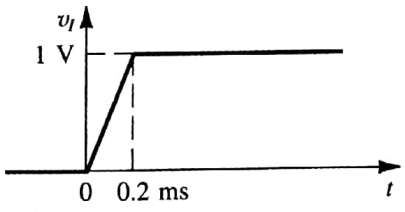


Figure P2.89

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

**2.90** An op-amp differentiator, employing the circuit shown in Fig. 2.27(a), has $R = 20\,\text{k}\Omega$ and $C = 0.1\,\mu\text{F}$. When a triangle wave of $\pm 1$-V peak amplitude at 1 kHz is applied to the input, what form of output results? What is its frequency? What is its peak amplitude? What is its average value? What value of $R$ is needed to cause the output to have a 12-V peak amplitude?

**2.91** Use an ideal op amp to design a differentiation circuit for which the time constant is $10^{-3}$ s using a 10-nF capacitor. What are the gains and phase shifts found for this circuit at one-tenth and 10 times the unity-gain frequency? A series input resistor is added to limit the gain magnitude at high frequencies to 100 V/V. What is the associated 3-dB frequency? What gain and phase shift result at 10 times the unity-gain frequency?

**D 2.92** Figure P2.92 shows a circuit that performs the high-pass, single-time-constant function. Such a circuit is known as a first-order high-pass active filter. Derive the transfer function and show that the high-frequency gain is $(-R_2/R_1)$ and the 3-dB frequency $\omega_0 = 1/CR_1$. Design the circuit to obtain a high-frequency input resistance of 1 kΩ, a high-frequency gain of 40 dB, and a 3-dB frequency of 2 kHz. At what frequency does the magnitude of the transfer function reduce to unity?

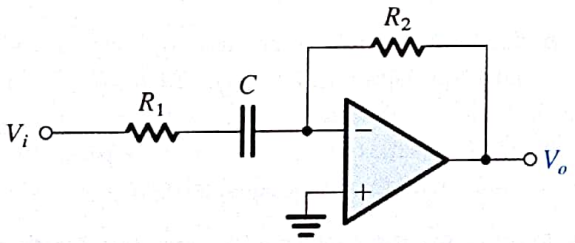


Figure P2.92

**D **2.93** Derive the transfer function of the circuit in Fig. P2.93 (for an ideal op amp) and show that it can be written in the form

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{[1+(\omega_1/j\omega)][1+j(\omega/\omega_2)]}$$

where $\omega_1 = 1/C_1R_1$ and $\omega_2 = 1/C_2R_2$. Assuming that the circuit is designed such that $\omega_2 \gg \omega_1$, find approximate expressions for the transfer function in the following frequency regions:

(a) $\omega \ll \omega_1$
(b) $\omega_1 \ll \omega \ll \omega_2$
(c) $\omega \gg \omega_2$

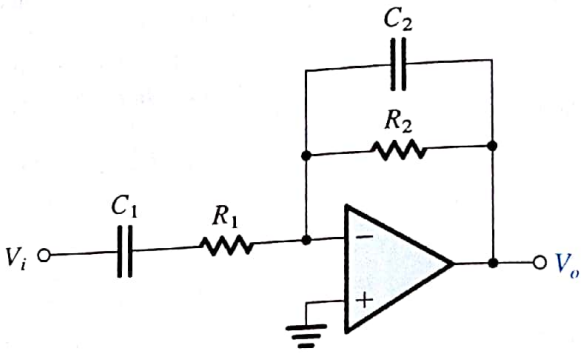


Figure P2.93

Use these approximations to sketch a Bode plot for the magnitude response. Observe that the circuit performs as an amplifier whose gain rolls off at the low-frequency end in the manner of a high-pass STC network, and at the high-frequency end in the manner of a low-pass STC network. Design the circuit to provide a gain of 40 dB in the "middle-frequency range," a low-frequency 3-dB point at 200 Hz, a high-frequency 3-dB point at 200 kHz, and an input resistance (at $\omega \gg \omega_1$) of 2 kΩ.

## Section 2.6: DC Imperfections

**2.94** An op amp wired in the inverting configuration with the input grounded, having $R_2 = 100\,\text{k}\Omega$ and $R_1 = 2\,\text{k}\Omega$, has an output dc voltage of $-0.2$ V. If the input bias current is known to be very small, find the input offset voltage.

**2.95** A noninverting amplifier with a gain of 100 uses an op amp having an input offset voltage of $\pm 2$ mV. Find the output when the input is $0.01 \sin \omega t$, volts.

**2.96** A noninverting amplifier with a closed-loop gain of 1000 is designed using an op amp having an input offset voltage of 3 mV and output saturation levels of $\pm 12$ V. What is the maximum amplitude of the sine wave that can be applied at the input without the output clipping? If the amplifier is

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either +1.0 V/V or +2.0 V/V simply by short-circuiting a single resistor in each case?

**D 2.46** Figure P2.46 shows a circuit for an analog voltmeter of very high input resistance that uses an inexpensive moving-coil meter. The voltmeter measures the voltage $V$ applied between the op amp's positive-input terminal and ground. Assuming that the moving coil produces full-scale deflection when the current passing through it is 100 μA, find the value of $R$ such that a full-scale reading is obtained when $V$ is +10 V. Does the meter resistance shown affect the voltmeter calibration?

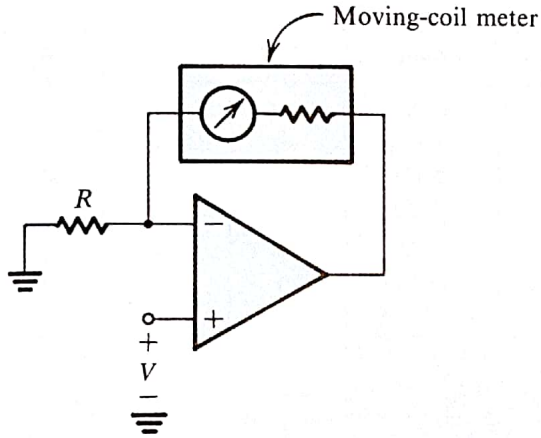


Figure P2.46

**D *2.47** (a) Use superposition to show that the output of the circuit in Fig. P2.47 is given by

$$v_O = \left[\frac{R_f}{R_{N1}}v_{N1} + \frac{R_f}{R_{N2}}v_{N2} + \cdots + \frac{R_f}{R_{Nn}}v_{Nn}\right] + \left[1 + \frac{R_f}{R_N}\right]\left[\frac{R_P}{R_{P1}}v_{P1} + \frac{R_P}{R_{P2}}v_{P2} + \cdots + \frac{R_P}{R_{Pn}}v_{Pn}\right]$$

where $R_N = R_{N1} \| R_{N2} \| \cdots \| R_{Nn}$, and

$$R_P = R_{P1} \| R_{P2} \| \cdots \| R_{Pn} \| R_{P0}$$

(b) Design a circuit to obtain

$$v_O = -4v_{N1} + v_{P1} + 3v_{P2}$$

The smallest resistor used should be 10 kΩ.

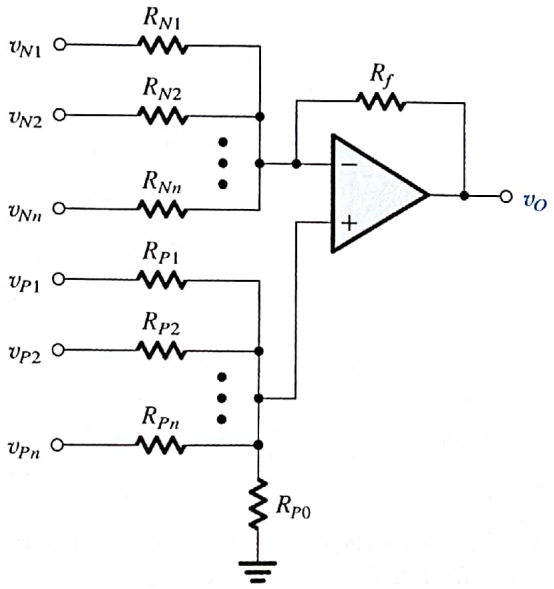


Figure P2.47

**D *2.48** Design a circuit, using one ideal op amp, whose output is $v_O = v_{I1} + 2v_{I2} - 9v_{I3} + 4v_{I4}$. (*Hint:* Use a structure similar to that shown in general form in Fig. P2.47.)

**2.49** Derive an expression for the voltage gain, $v_O/v_I$, of the circuit in Fig. P2.49.

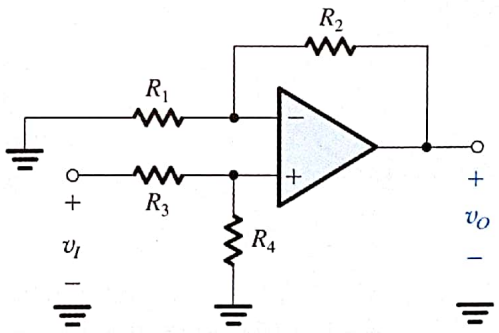


Figure P2.49

**2.50** For the circuit in Fig. P2.50, use superposition to find $v_O$ in terms of the input voltages $v_1$ and $v_2$. Assume an ideal op amp. For

$$v_1 = 10\sin(2\pi \times 60t) - 0.1\sin(2\pi \times 1000t), \text{ volts}$$
$$v_2 = 10\sin(2\pi \times 60t) + 0.1\sin(2\pi \times 1000t), \text{ volts}$$

find $v_O$.

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

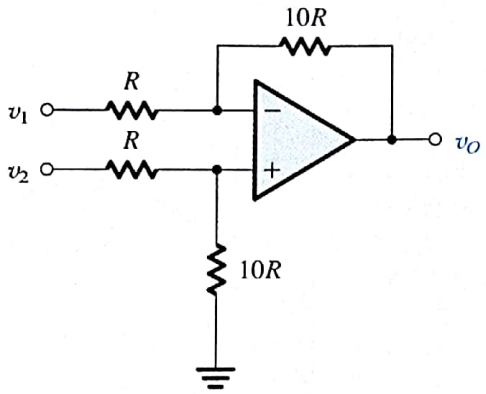


Figure P2.50

**D 2.51** The circuit shown in Fig. P2.51 utilizes a 10-kΩ potentiometer to realize an adjustable-gain amplifier. Derive an expression for the gain as a function of the potentiometer setting $x$. Assume the op amp to be ideal. What is the range of gains obtained? Show how to add a fixed resistor so that the gain range can be 1 to 11 V/V. What should the resistor value be?

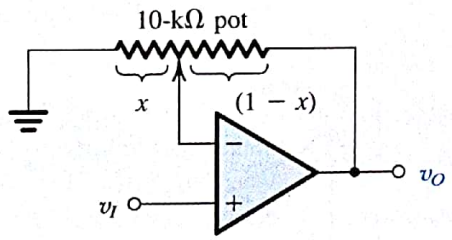


Figure P2.51

**D 2.52** Given the availability of resistors of value 1 kΩ and 10 kΩ only, design a circuit based on the noninverting configuration to realize a gain of +10 V/V. What is the input resistance of your amplifier?

**2.53** It is required to connect a 10-V source with a source resistance of 1 MΩ to a 1-kΩ load. Find the voltage that will appear across the load if:

(a) The source is connected directly to the load.
(b) A unity-gain op-amp buffer is inserted between the source and the load.

In each case find the load current and the current supplied by the source. Where does the load current come from in case (b)?

**2.54** Derive an expression for the gain of the voltage follower of Fig. 2.14, assuming the op amp to be ideal except for having a finite gain $A$. Calculate the value of the closed-loop gain for $A = 1000$, 100, and 10. In each case find the percentage error in gain magnitude from the nominal value of unity.

**2.55** Complete the following table for feedback amplifiers created using one ideal op amp. Note that $R_{in}$ signifies input resistance and $R_1$ and $R_2$ are feedback-network resistors as labeled in the inverting and noninverting configurations.

| Case | Gain | $R_{in}$ | $R_1$ | $R_2$ |
|---|---|---|---|---|
| a | −10 V/V | 10 kΩ | | |
| b | −1 V/V | | 100 kΩ | |
| c | −2 V/V | | | 200 kΩ |
| d | +1 V/V | ∞ | | |
| e | +2 V/V | | 100 kΩ | |
| f | +11 V/V | | | 100 kΩ |
| g | −0.5 V/V | 20 kΩ | | |

**D 2.56** A noninverting op-amp circuit with nominal gain of 10 V/V uses an op amp with open-loop gain of 100 V/V and a lowest-value resistor of 10 kΩ. What closed-loop gain actually results? With what value resistor can which resistor be shunted to achieve the nominal gain? If in the manufacturing process, an op amp of gain 200 V/V were used, what closed-loop gain would result in each case (the uncompensated one, and the compensated one)?

**2.57** Use Eq. (2.11) to show that if the reduction in the closed-loop gain $G$ from the nominal value $G_0 = 1 + R_2/R_1$ is to be kept less than $x\%$ of $G_0$, then the open-loop gain of the op amp must exceed $G_0$ by at least a factor $F = (100/x) - 1 \simeq 100/x$. Find the required $F$ for $x = 0.01$, 0.1, 1, and 10. Utilize these results to find for each value of $x$ the minimum required open-loop gain to obtain closed-loop gains of 1, 10, $10^2$, $10^3$, and $10^4$ V/V.

**2.58** For each of the following combinations of op-amp open-loop gain $A$ and nominal closed-loop gain $G_0$, calculate the actual closed-loop gain $G$ that is achieved. Also, calculate the percentage by which $|G|$ falls short of the nominal gain magnitude $|G_0|$.

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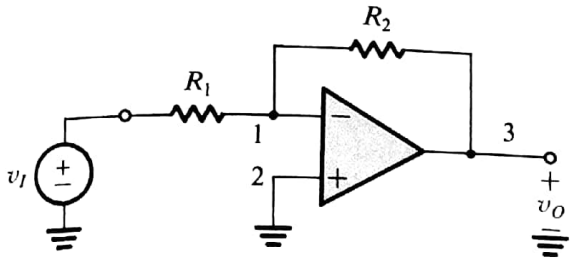


**Figure 2.5** The inverting closed-loop configuration.

with a voltage $v_I$. The output of the overall circuit is taken at terminal 3 (i.e., between terminal 3 and ground). Terminal 3 is, of course, a convenient point from which to take the output, since the impedance level there is ideally zero. Thus the voltage $v_O$ will not depend on the value of the current that might be supplied to a load impedance connected between terminal 3 and ground.

## 2.2.1 The Closed-Loop Gain

We now wish to analyze the circuit in Fig. 2.5 to determine the **closed-loop gain** $G$, defined as

$$G \equiv \frac{v_O}{v_I}$$

We will do so assuming the op amp to be ideal. Figure 2.6(a) shows the equivalent circuit, and the analysis proceeds as follows: The gain $A$ is very large (ideally infinite). If we assume that the circuit is "working" and producing a finite output voltage at terminal 3, then the voltage between the op-amp input terminals should be negligibly small and ideally zero. Specifically, if we call the output voltage $v_O$, then, by definition,

$$v_2 - v_1 = \frac{v_O}{A} = 0$$

It follows that the voltage at the inverting input terminal ($v_1$) is given by $v_1 = v_2$. That is, because the gain $A$ approaches infinity, the voltage $v_1$ approaches and ideally equals $v_2$. We speak of this as the two input terminals "tracking each other in potential." We also speak of a "virtual short circuit" that exists between the two input terminals. Here the word *virtual* should be emphasized, and one should *not* make the mistake of physically shorting terminals 1 and 2 together while analyzing a circuit. A **virtual short circuit** means that whatever voltage is at 2 will automatically appear at 1 because of the infinite gain $A$. But terminal 2 happens to be connected to ground; thus $v_2 = 0$ and $v_1 = 0$. We speak of terminal 1 as being a **virtual ground**—that is, having zero voltage but not physically connected to ground.

Now that we have determined $v_1$ we are in a position to apply Ohm's law and find the current $i_1$ through $R_1$ (see Fig. 2.6) as follows:

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1}$$

Where will this current go? It cannot go into the op amp, since the ideal op amp has an infinite input impedance and hence draws zero current. It follows that $i_1$ will have to flow through $R_2$ to the low-impedance terminal 3. We can then apply Ohm's law to $R_2$ and determine $v_O$; that is,

$$\begin{aligned} v_O &= v_1 - i_1 R_2 \\ &= 0 - \frac{v_I}{R_1} R_2 \end{aligned}$$

Thus,

$$\frac{v_O}{v_I} = -\frac{R_2}{R_1}$$