PROBLEM SET #11

Issued: Tuesday, November 20, 2018 (Updated 11/27/18)

Due: Tuesday, December 4, 2018, at 12:00 noon via Gradescope.

1. Sedra & Smith, Problem 8.65
2. Sedra & Smith, Problem 10.73
3. What are the Q-points $[I_D, V_{DS}]$ for the transistors in the amplifier in Figure PS11.1 given the parameters in table PS11.1 below? Find the differential-mode gain A_{dm} $\left(\frac{v_{od}}{v_{id}}\right)$, common-mode gain A_{cm} $\left(\frac{v_{ocm}}{v_{icm}}\right)$, CMRR (common-mode rejection ratio, $\left|\frac{A_{dm}}{A_{cm}}\right|$), and differential-mode and common-mode input resistances.

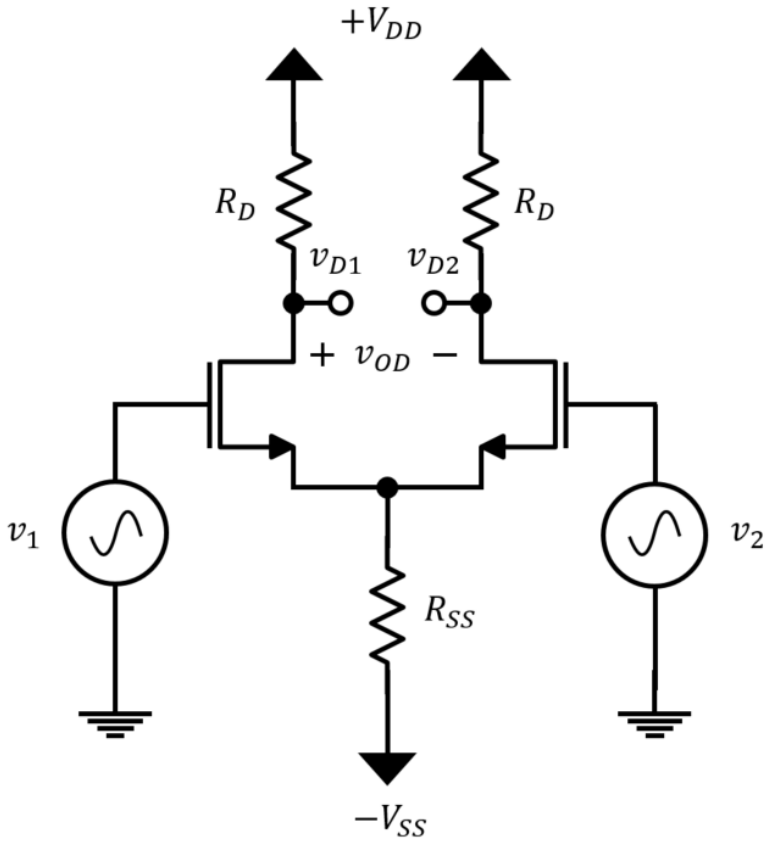

Figure PS11.1

PARAMETER	*VALUE*	*UNIT*
k_n	400	μA/V^2
V_{tn}	1	V
V_{DD}	12	V
V_{SS}	12	V
R_{SS}	220	kΩ
R_D	330	kΩ

Table PS11.1

4. What are the rise time, fall time and propagation delay for a minimum size CMOS inverter with the parameters given in Table PS11.2 in which both *W/L* ratios are 2/1? Assume a load capacitance of 0.5 pF and $V_{DD} = 3.3$ V.

5. What are the sizes of the transistors in the CMOS inverter with the parameters given in Table PS11.2 if it must drive a 1-pF capacitance with an average propagation delay of 3 ns? Design the inverter for equal rise and fall times. Assume $V_{DD} = 5$ V.

6. Design a symmetrical CMOS reference inverter to provide a delay of 1 ns when driving a 10-pF load for (a) $V_{DD} = 5$ V and (b) $V_{DD} = 3.3$ V. Assume $V_{tn} = -V_{tp} = 0.7$ V.

7. What are the noise margins of a minimum size CMOS inverter in which both *W/L* ratios are 2/1, the transistors have the parameters given in Table PS11.2, and $V_{DD} = 5$ V?

8. What are the noise margins for a symmetrical CMOS inverter operating with $V_{DD} = 3.3$ V and $V_{tn} = -V_{tp} = 0.75$ V?

9. What are the noise margins for a CMOS inverter having $(W/L)_N = (W/L)_P$ operating with $V_{DD} = 3.3$ V and $V_{tn} = -V_{tp} = 0.75$ V?

PARAMETER	*VALUE*	*UNIT*
k'_n	25	μA/V^2
k'_p	10	μA/V^2
V_{tn}	1	V
V_{tp}	-1	V

Table PS11.2

10. One method to estimate the average propagation delay of an inverter is to construct a long ring of inverters, as shown in Figure PS11.2. This circuit is called a *ring oscillator*, and the output of any inverter in the chain will be similar to a square wave.

(a) Suppose that the chain contains 301 inverters and the average propagation delay of an inverter is 100 ps. What will the period of the square wave generated by the oscillator be?

(b) Why should the number of inverters be odd? What could happen if an even number of inverters were used in the ring oscillator?

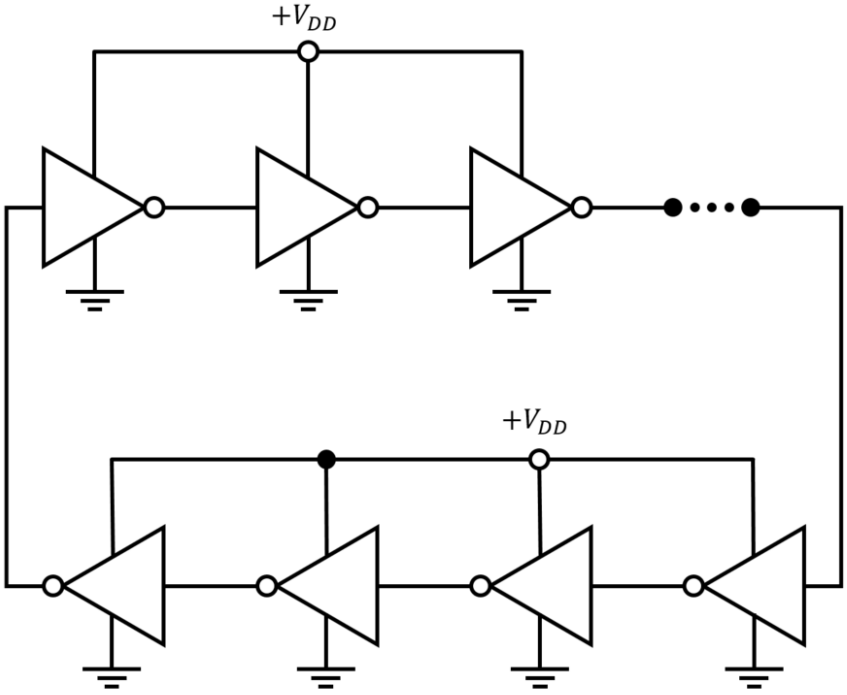

Figure PS10.2