

- (a) Assuming ideal op amps, sketch the voltage waveforms at nodes B and C for a 1-V peak-to-peak sine wave applied at A. Also sketch v_o .
- (b) What is the voltage gain v_o/v_i ?
- (c) Assuming that the op amps operate from ± 15 -V power supplies and that their output saturates at ± 14 V (in the manner shown in Fig. 1.14), what is the largest sine-wave output that can be accommodated? Specify both its peak-to-peak and rms values.

*2.78 The two circuits in Fig. P2.78 are intended to function as voltage-to-current converters; that is, they supply the load impedance Z_L with a current proportional to v_i and independent of the value of Z_L . Show that this is indeed the case, and find for each circuit i_o as a function of v_i . Comment on the differences between the two circuits.

Section 2.5: Integrators and Differentiators

2.79 A Miller integrator incorporates an ideal op amp, a resistor R of 10 k Ω , and a capacitor C of 1 nF. A sine-wave signal is applied to its input.

- (a) At what frequency (in Hz) are the input and output signals equal in amplitude?
- (b) At that frequency, how does the phase of the output sine wave relate to that of the input?

- (c) If the frequency is lowered by a factor of 10 from that found in (a), by what factor does the output voltage change, and in what direction (smaller or larger)?
- (d) What is the phase relation between the input and output in situation (c)?

D 2.80 Design a Miller integrator with a time constant of 1 s and an input resistance of 100 k Ω . A dc voltage of -1 volt is applied at the input at time 0, at which moment $v_o = -10$ V. How long does it take the output to reach 0 V? $+10$ V?

2.81 An op-amp-based inverting integrator is measured at 10 kHz to have a voltage gain of -100 V/V. At what frequency is its gain reduced to -1 V/V? What is the integrator time constant?

D 2.82 Design a Miller integrator that has a unity-gain frequency of 10 krad/s and an input resistance of 100 k Ω . Sketch the output you would expect for the situation in which, with output initially at 0 V, a 2-V, 100- μ s pulse is applied to the input. Characterize the output that results when a sine wave $2 \sin 10^4 t$ is applied to the input.

D 2.83 Design a Miller integrator whose input resistance is 10 k Ω and unity-gain frequency is 100 kHz. What components are needed? For long-term stability, a feedback resistor is introduced across the capacitor to limit the dc gain

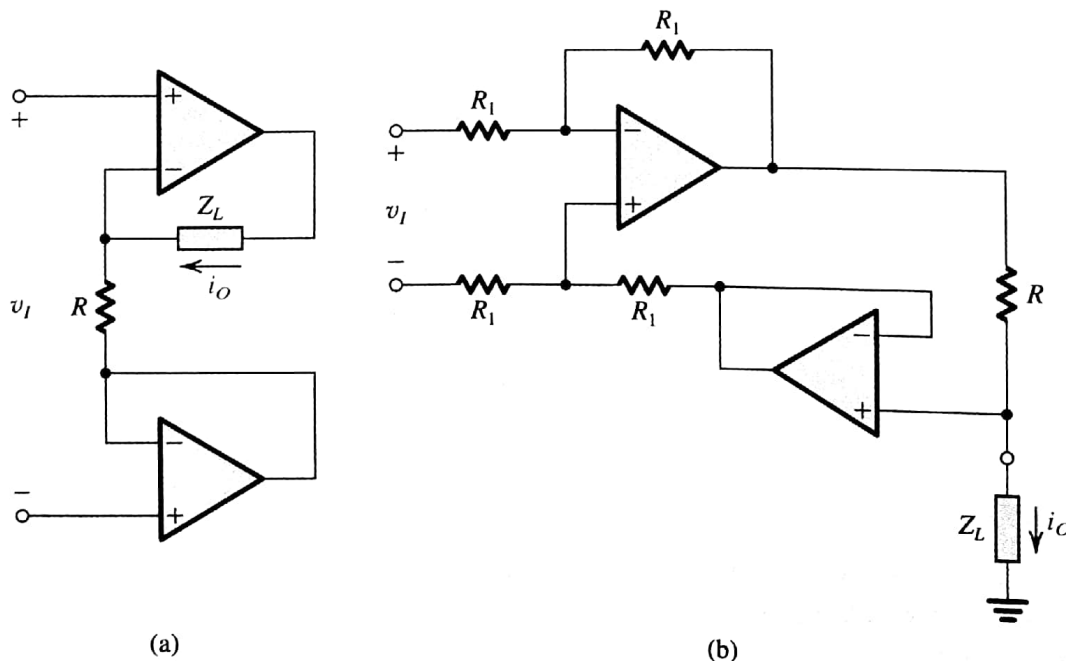


Figure P2.78

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

to 40 dB. What is its value? What is the associated lower 3-dB frequency? Sketch and label the output that results with a 10- μ s, 1-V positive-input pulse (initially at 0 V) with (a) no dc stabilization (but with the output initially at 0 V) and (b) the feedback resistor connected.

*2.84 A Miller integrator whose input and output voltages are initially zero and whose time constant is 1 ms is driven by the signal shown in Fig. P2.84. Sketch and label the output waveform that results. Indicate what happens if the input levels are ± 2 V, with the time constant the same (1 ms) and with the time constant raised to 2 ms.

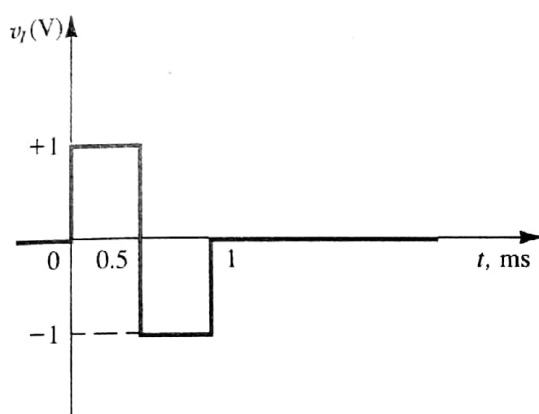


Figure P2.84

2.85 Consider a Miller integrator having a time constant of 1 ms and an output that is initially zero, when fed with a string of pulses of 10- μ s duration and 1-V amplitude rising from 0 V (see Fig. P2.85). Sketch and label the output waveform resulting. How many pulses are required for an output voltage change of 1 V?

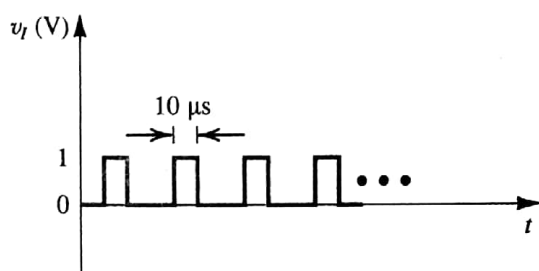


Figure P2.85

D 2.86 Figure P2.86 shows a circuit that performs a low-pass STC function. Such a circuit is known as a first-order,

low-pass active filter. Derive the transfer function and show that the dc gain is $(-R_2/R_1)$ and the 3-dB frequency $\omega_0 = 1/CR_2$. Design the circuit to obtain an input resistance of 10 k Ω , a dc gain of 40 dB, and a 3-dB frequency of 1 kHz. At what frequency does the magnitude of the transfer function reduce to unity?

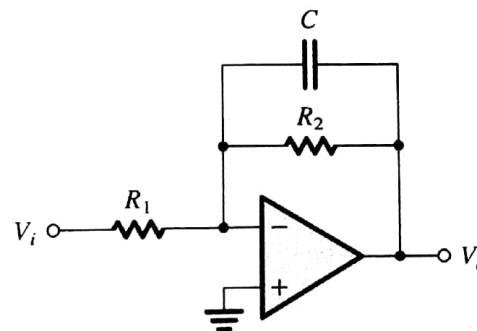


Figure P2.86

*2.87 Show that a Miller integrator implemented with an op amp with open-loop gain A_0 has a low-pass STC transfer function. What is the pole frequency of the STC function? How does this compare with the pole frequency of the ideal integrator? If an ideal Miller integrator is fed with a -1 -V pulse signal with a width $T = CR$, what will the output voltage be at $t = T$? Assume that at $t = 0, v_o = 0$. Repeat for an integrator with an op amp having $A_0 = 1000$.

2.88 A differentiator utilizes an ideal op amp, a 10-k Ω resistor, and a 1-nF capacitor. What is the frequency f_0 (in Hz) at which its input and output sine-wave signals have equal magnitude? What is the output signal for a 1-V peak-to-peak sine-wave input with frequency equal to $10f_0$?

2.89 An op-amp differentiator with 1-ms time constant is driven by the rate-controlled step shown in Fig. P2.89. Assuming v_o to be zero initially, sketch and label its waveform.

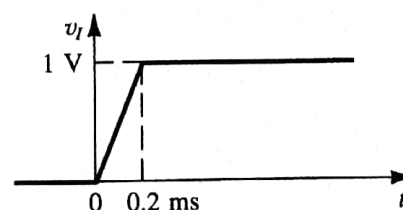


Figure P2.89

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

2.90 An op-amp differentiator, employing the circuit shown in Fig. 2.27(a), has $R = 20 \text{ k}\Omega$ and $C = 0.1 \text{ }\mu\text{F}$. When a triangle wave of $\pm 1\text{-V}$ peak amplitude at 1 kHz is applied to the input, what form of output results? What is its frequency? What is its peak amplitude? What is its average value? What value of R is needed to cause the output to have a 12-V peak amplitude?

2.91 Use an ideal op amp to design a differentiation circuit for which the time constant is 10^{-3} s using a 10-nF capacitor. What are the gains and phase shifts found for this circuit at one-tenth and 10 times the unity-gain frequency? A series input resistor is added to limit the gain magnitude at high frequencies to 100 V/V . What is the associated 3-dB frequency? What gain and phase shift result at 10 times the unity-gain frequency?

D 2.92 Figure P2.92 shows a circuit that performs the high-pass, single-time-constant function. Such a circuit is known as a first-order high-pass active filter. Derive the transfer function and show that the high-frequency gain is $(-R_2/R_1)$ and the 3-dB frequency $\omega_0 = 1/CR_1$. Design the circuit to obtain a high-frequency input resistance of $1 \text{ k}\Omega$, a high-frequency gain of 40 dB , and a 3-dB frequency of 2 kHz . At what frequency does the magnitude of the transfer function reduce to unity?

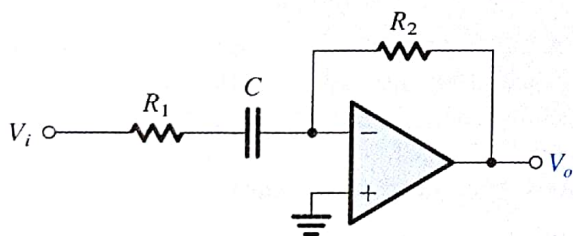


Figure P2.92

D **2.93 Derive the transfer function of the circuit in Fig. P2.93 (for an ideal op amp) and show that it can be written in the form

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{[1 + (\omega_1/j\omega)][1 + j(\omega/\omega_2)]}$$

where $\omega_1 = 1/C_1R_1$ and $\omega_2 = 1/C_2R_2$. Assuming that the circuit is designed such that $\omega_2 \gg \omega_1$, find approximate expressions

for the transfer function in the following frequency regions:

- (a) $\omega \ll \omega_1$
- (b) $\omega_1 \ll \omega \ll \omega_2$
- (c) $\omega \gg \omega_2$

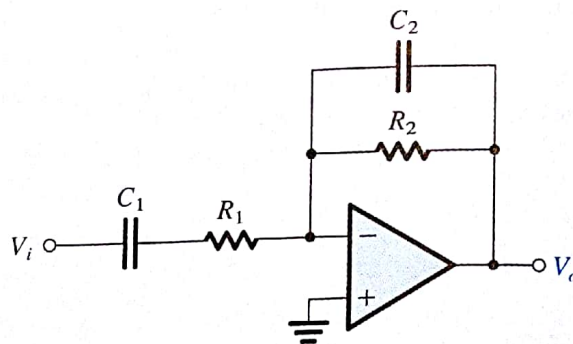


Figure P2.93

Use these approximations to sketch a Bode plot for the magnitude response. Observe that the circuit performs as an amplifier whose gain rolls off at the low-frequency end in the manner of a high-pass STC network, and at the high-frequency end in the manner of a low-pass STC network. Design the circuit to provide a gain of 40 dB in the “middle-frequency range,” a low-frequency 3-dB point at 200 Hz , a high-frequency 3-dB point at 200 kHz , and an input resistance (at $\omega \gg \omega_1$) of $2 \text{ k}\Omega$.

Section 2.6: DC Imperfections

2.94 An op amp wired in the inverting configuration with the input grounded, having $R_2 = 100 \text{ k}\Omega$ and $R_1 = 2 \text{ k}\Omega$, has an output dc voltage of -0.2 V . If the input bias current is known to be very small, find the input offset voltage.

2.95 A noninverting amplifier with a gain of 100 uses an op amp having an input offset voltage of $\pm 2 \text{ mV}$. Find the output when the input is $0.01 \sin \omega t$, volts.

2.96 A noninverting amplifier with a closed-loop gain of 1000 is designed using an op amp having an input offset voltage of 3 mV and output saturation levels of $\pm 12 \text{ V}$. What is the maximum amplitude of the sine wave that can be applied at the input without the output clipping? If the amplifier is

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem