Table P3.11

Doping Concentration (carriers/cm^3)	μ_n (cm^2/V · s)	μ_p (cm^2/V · s)	D_n (cm^2/s)	D_p (cm^2/s)
Intrinsic	1350	480		
10^{16}	1200	400		
10^{17}	750	260		
10^{18}	380	160		

Section 3.4: The *pn* Junction

3.12 Calculate the built-in voltage of a junction in which the p and n regions are doped equally with 5×10^{16} atoms/cm^3. Assume $n_i = 1.5 \times 10^{10}$/cm^3. With the terminals left open, what is the width of the depletion region, and how far does it extend into the p and n regions? If the cross-sectional area of the junction is 20 μm^2, find the magnitude of the charge stored on either side of the junction.

3.13 If, for a particular junction, the acceptor concentration is 10^{17}/cm^3 and the donor concentration is 10^{16}/cm^3, find the junction built-in voltage. Assume $n_i = 1.5 \times 10^{10}$/cm^3. Also, find the width of the depletion region (W) and its extent in each of the p and n regions when the junction terminals are left open. Calculate the magnitude of the charge stored on either side of the junction. Assume that the junction area is 100 μm^2.

3.14 Estimate the total charge stored in a 0.1-μm depletion layer on one side of a 10-μm × 10-μm junction. The doping concentration on that side of the junction is 10^{18}/cm^3.

3.15 In a *pn* junction for which $N_A \gg N_D$, and the depletion layer exists mostly on the shallowly doped side with $W = 0.2$ μm, find V_0 if $N_D = 10^{16}$/cm^3. Also calculate Q_J for the case $A = 10$ μm^2.

3.16 By how much does V_0 change if N_A or N_D is increased by a factor of 10?

Section 3.5: The *pn* Junction with an Applied Voltage

3.17 If a 3-V reverse-bias voltage is applied across the junction specified in Problem 3.13, find W and Q_J.

3.18 Show that for a *pn* junction reverse-biased with a voltage V_R, the depletion-layer width W and the charge stored on either side of the junction, Q_J, can be expressed as

$$W = W_0\sqrt{1+\frac{V_R}{V_0}}$$

$$Q_J = Q_{J0}\sqrt{1+\frac{V_R}{V_0}}$$

where W_0 and Q_{J0} are the values in equilibrium.

3.19 In a forward-biased *pn* junction show that the ratio of the current component due to hole injection across the junction to the component due to electron injection is given by

$$\frac{I_p}{I_n} = \frac{D_p}{D_n}\frac{L_n}{L_p}\frac{N_A}{N_D}$$

Evaluate this ratio for the case $N_A = 10^{18}$/cm^3, $N_D = 10^{16}$/cm^3, $L_p = 5$ μm, $L_n = 10$ μm, $D_p = 10$ cm^2/s, and $D_n = 20$ cm^2/s, and hence find I_p and I_n for the case in which the *pn* junction is conducting a forward current $I = 100$ μA.

3.20 Calculate I_S and the current I for $V = 750$ mV for a *pn* junction for which $N_A = 10^{17}$/cm^3, $N_D = 10^{16}$/cm^3, $A = 100$ μm^2, $n_i = 1.5 \times 10^{10}$/cm^3, $L_p = 5$ μm, $L_n = 10$ μm, $D_p = 10$ cm^2/s, and $D_n = 18$ cm^2/s.

3.21 Assuming that the temperature dependence of I_S arises mostly because I_S is proportional to n_i^2, use the expression for n_i in Eq. (3.2) to determine the factor by which n_i^2 changes as T changes from 300 K to 305 K. This will be approximately the same factor by which I_S changes for a 5°C rise in temperature. What is the factor?

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

(a) Provide a rough estimate of the diode current you would expect.
(b) Estimate the diode current more closely using iterative analysis.

D 4.37 Assuming the availability of diodes for which $v_D = 0.75$ V at $i_D = 1$ mA, design a circuit that utilizes four diodes connected in series, in series with a resistor R connected to a 15-V power supply. The voltage across the string of diodes is to be 3.3 V.

4.38 A diode operates in a series circuit with a resistance R and a dc source V. A designer, considering using a constant-voltage model, is uncertain whether to use 0.7 V or 0.6 V for V_D. For what value of V is the difference in the calculated values of current only 1%? For $V = 3$ V and $R = 1$ kΩ, what two current estimates would result from the use of the two values of V_D? What is their percentage difference?

4.39 A designer has a supply of diodes for which a current of 2 mA flows at 0.7 V. Using a 1-mA current source, the designer wishes to create a reference voltage of 1.3 V. Suggest a combination of series and parallel diodes that will do the job as well as possible. How many diodes are needed? What voltage is actually achieved?

4.40 Solve the problems in Example 4.2 using the constant-voltage-drop ($V_D = 0.7$ V) diode model.

4.41 For the circuits shown in Fig. P4.2, using the constant-voltage-drop ($V_D = 0.7$ V) diode model, find the voltages and currents indicated.

4.42 For the circuits shown in Fig. P4.3, using the constant-voltage-drop ($V_D = 0.7$ V) diode model, find the voltages and currents indicated.

4.43 For the circuits in Fig. P4.9, using the constant-voltage-drop ($V_D = 0.7$ V) diode model, find the values of the labeled currents and voltages.

4.44 For the circuits in Fig. P4.10, utilize Thévenin's theorem to simplify the circuits and find the values of the labeled currents and voltages. Assume that conducting diodes can be represented by the constant-voltage-drop model ($V_D = 0.7$ V).

D 4.45 Repeat Problem 4.11, representing the diode by the constant-voltage-drop ($V_D = 0.7$ V) model. How different is the resulting design?

4.46 The small-signal model is said to be valid for voltage variations of about 5 mV. To what percentage current change does this correspond? (Consider both positive and negative signals.) What is the maximum allowable voltage signal (positive or negative) if the current change is to be limited to 10%?

4.47 In a particular circuit application, ten "20-mA diodes" (a 20-mA diode is a diode that provides a 0.7-V drop when the current through it is 20 mA) connected in parallel operate at a total current of 0.1 A. For the diodes closely matched, what current flows in each? What is the corresponding small-signal resistance of each diode and of the combination? Compare this with the incremental resistance of a single diode conducting 0.1 A. If each of the 20-mA diodes has a series resistance of 0.2 Ω associated with the wire bonds to the junction, what is the equivalent resistance of the 10 parallel-connected diodes? What connection resistance would a single diode need in order to be totally equivalent? (*Note:* This is why the parallel connection of real diodes can often be used to advantage.)

4.48 In the circuit shown in Fig. P4.48, I is a dc current and v_s is a sinusoidal signal. Capacitors C_1 and C_2 are very large; their function is to couple the signal to and from the diode but block the dc current from flowing into the signal source or the load (not shown). Use the diode small-signal model to show that the signal component of the output voltage is

$$v_o = v_s \frac{V_T}{V_T + IR_s}$$

If $v_s = 10$ mV, find v_o for $I = 1$ mA, 0.1 mA, and 1 μA. Let $R_s = 1$ kΩ. At what value of I does v_o become one-half of v_s? Note that this circuit functions as a signal attenuator with the attenuation factor controlled by the value of the dc current I.

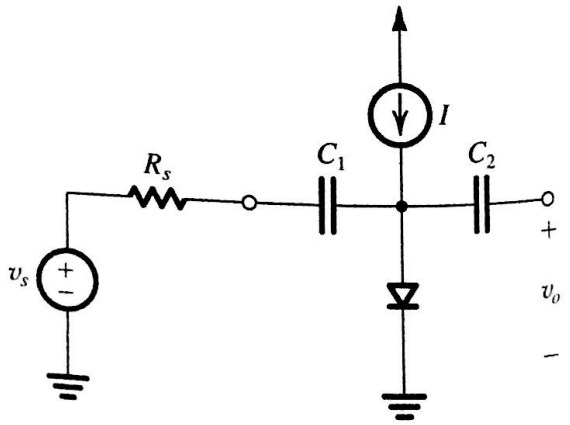

Figure P4.48

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging

5.19 A particular n-channel MOSFET is measured to have a drain current of 0.4 mA at $V_{GS} = V_{DS} = 1$ V and of 0.1 mA at $V_{GS} = V_{DS} = 0.8$ V. What are the values of k_n and V_t for this device?

D 5.20 For a particular IC-fabrication process, the transconductance parameter $k_n' = 400\ \mu A/V^2$, and $V_t = 0.5$ V. In an application in which $v_{GS} = v_{DS} = V_{supply} = 1.8$ V, a drain current of 2 mA is required of a device of minimum length of 0.18 μm. What value of channel width must the design use?

5.21 An NMOS transistor, operating in the linear-resistance region with $v_{DS} = 50$ mV, is found to conduct 25 μA for $v_{GS} = 1$ V and 50 μA for $v_{GS} = 1.5$ V. What is the apparent value of threshold voltage V_t? If $k_n' = 50\ \mu A/V^2$, what is the device W/L ratio? What current would you expect to flow with $v_{GS} = 2$ V and $v_{DS} = 0.1$ V? If the device is operated at $v_{GS} = 2$ V, at what value of v_{DS} will the drain end of the MOSFET channel just reach pinch-off, and what is the corresponding drain current?

5.22 For an NMOS transistor, for which $V_t = 0.4$ V, operating with v_{GS} in the range of 1.0 V to 1.8 V, what is the largest value of v_{DS} for which the channel remains continuous?

5.23 An NMOS transistor, fabricated with $W = 20$ μm and $L = 1$ μm in a technology for which $k_n' = 100\ \mu A/V^2$ and $V_t = 0.8$ V, is to be operated at very low values of v_{DS} as a linear resistor. For v_{GS} varying from 1.0 V to 4.8 V, what range of resistor values can be obtained? What is the available range if

(a) the device width is halved?
(b) the device length is halved?
(c) both the width and length are halved?

5.24 When the drain and gate of a MOSFET are connected together, a two-terminal device known as a "diode-connected transistor" results. Figure P5.24 shows such devices obtained from MOS transistors of both polarities. Show that

(a) the i–v relationship is given by

$$i = \frac{1}{2}k'\frac{W}{L}(v - |V_t|)^2$$

(b) the incremental resistance r for a device biased to operate at $v = |V_t| + V_{OV}$ is given by

$$r \equiv 1\Big/\left[\frac{\partial i}{\partial v}\right] = 1\Big/\left(k'\frac{W}{L}V_{OV}\right)$$

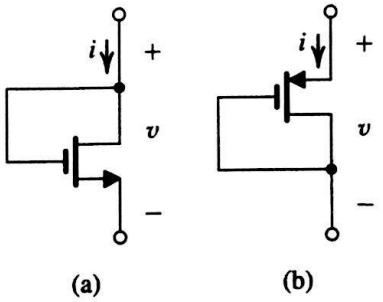

Figure P5.24

5.25 For the circuit in Fig. P5.25, sketch i_D versus v_S for v_S varying from 0 to V_{DD}. Clearly label your sketch.

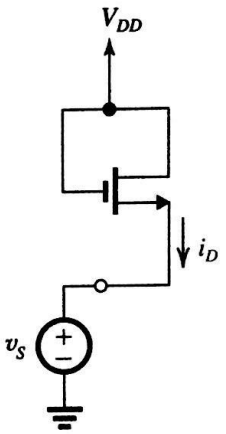

Figure P5.25

5.26 For the circuit in Fig. P5.26, find an expression for v_{DS} in terms of i_D. Sketch and clearly label a graph for v_{DS} versus i_D.

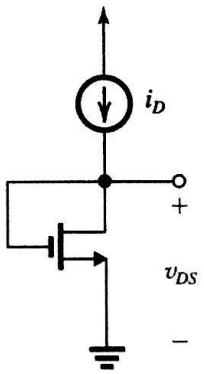

Figure P5.26

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

Case	Voltage (V)						Region of operation
	V_S	V_G	V_D	V_{GS}	V_{OV}	V_{DS}	
a	+1.0	+1.0	+2.0				
b	+1.0	+2.5	+2.0				
c	+1.0	+2.5	+1.5				
d	+1.0	+1.5	0				
e	0	+2.5	+1.0				
f	+1.0	+1.0	+1.0				
g	−1.0	0	0				
h	−1.5	0	0				
i	−1.0	0	+1.0				
j	+0.5	+2.0	+0.5				

***5.27** The table above lists 10 different cases labeled (a) to (j) for operating an NMOS transistor with $V_t = 1$ V. In each case the voltages at the source, gate, and drain (relative to the circuit ground) are specified. You are required to complete the table entries. Note that if you encounter a case for which v_{DS} is negative, you should exchange the drain and source before solving the problem. You can do this because the MOSFET is a symmetric device.

5.28 The NMOS transistor in Fig. P5.28 has $V_t = 0.4$ V and $k_n'(W/L) = 1$ mA/V^2. Sketch and clearly label i_D versus v_G with v_G varying in the range 0 to +1.8 V. Give equations for the various portions of the resulting graph.

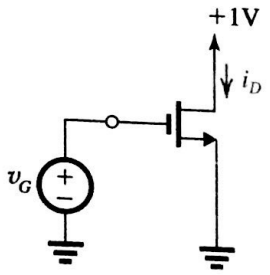

Figure P5.28

5.29 Figure P5.29 shows two NMOS transistors operating in saturation at equal V_{GS} and V_{DS}.

(a) If the two devices are matched except for a maximum possible mismatch in their W/L ratios of 3%, what is the maximum resulting mismatch in the drain currents?

(b) If the two devices are matched except for a maximum possible mismatch in their V_t values of 10 mV, what is the maximum resulting mismatch in the drain currents? Assume that the nominal value of V_t is 0.6 V.

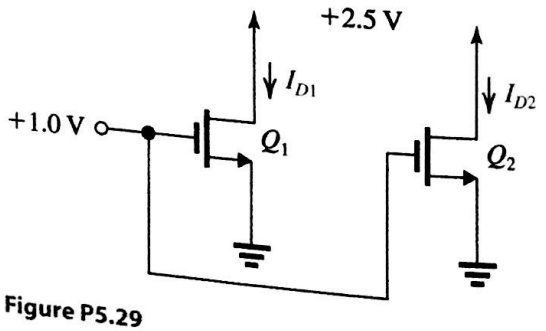

Figure P5.29

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

5.30 For a particular MOSFET operating in the saturation region at a constant v_{GS}, i_D is found to be 0.5 mA for $v_{DS} = 1$ V and 0.52 mA for $v_{DS} = 2$ V. What values of r_o, V_A, and λ correspond?

5.31 A particular MOSFET has $V_A = 20$ V. For operation at 0.1 mA and 1 mA, what are the expected output resistances? In each case, for a change in v_{DS} of 1 V, what percentage change in drain current would you expect?

D 5.32 In a particular IC design in which the standard channel length is 1 μm, an NMOS device with W/L of 10 operating at 200 μA is found to have an output resistance of 100 kΩ, about $\frac{1}{5}$ of that needed. What dimensional change can be made to solve the problem? What is the new device length? The new device width? The new W/L ratio? What is V_A for the standard device in this IC? The new device?

D 5.33 For a particular n-channel MOS technology, in which the minimum channel length is 0.5 μm, the associated value of λ is 0.03 V^{-1}. If a particular device for which L is 1.5 μm operates in saturation at $v_{DS} = 1$ V with a drain current of 100 μA, what does the drain current become if v_{DS} is raised to 5 V? What percentage change does this represent? What can be done to reduce the percentage by a factor of 2?

5.34 An NMOS transistor is fabricated in a 0.5-μm process having $k_n' = 200$ μA/V^2 and $V_A' = 20$ V/μm of channel length. If $L = 1.5$ μm and $W = 15$ μm, find V_A and λ. Find the value of I_D that results when the device is operated with an overdrive voltage of 0.5 V and $V_{DS} = 2$ V. Also, find the value of r_o at this operating point. If V_{DS} is increased by 1 V, what is the corresponding change in I_D?

5.35 If in an NMOS transistor, both W and L are quadrupled and V_{OV} is halved, by what factor does r_o change?

D 5.36 Consider the circuit in Fig. P5.29 with both transistors perfectly matched but with the dc voltage at the drain of Q_1 lowered to +2 V. If the two drain currents are to be matched within 1% (i.e., the maximum difference allowed between the two currents is 1%), what is the minimum required value of V_A? If the technology is specified to have $V_A' = 100$ V/μm, what is the minimum channel length the designer must use?

5.37 Complete the missing entries in the following table, which describes characteristics of suitably biased NMOS transistors:

MOS	1	2	3	4
λ (V^{-1})		0.02		
V_A (V)	20			100
I_D (mA)	0.5		0.1	
r_o (kΩ)		25	100	500

5.38 A PMOS transistor has $k_p'(W/L) = 100$ μA/V^2, $V_t = -1.0$ V, and $\lambda = -0.02$ V^{-1}. The gate is connected to ground and the source to +5 V. Find the drain current for $v_D = +4$ V, +2 V, +1 V, 0 V, and −5 V.

5.39 A p-channel transistor for which $|V_t| = 0.8$ V and $|V_A| = 40$ V operates in saturation with $|v_{GS}| = 3$ V, $|v_{DS}| = 4$ V, and $i_D = 3$ mA. Find corresponding signed values for v_{GS}, v_{SG}, v_{DS}, v_{SD}, V_t, V_A, λ, and $k_p'(W/L)$.

5.40 The table below lists the terminal voltages of a PMOS transistor in six cases, labeled a, b, c, d, e, and f. The transistor has $V_{tp} = -1$ V. Complete the table entries.

	V_S	V_G	V_D	V_{SG}	$\lvert V_{OV}\rvert$	V_{SD}	Region of operation
a	+2	+2	0				
b	+2	+1	0				
c	+2	0	0				
d	+2	0	+1				
e	+2	0	+1.5				
f	+2	0	+2				

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem