transistor β is specified to lie in the range 50 to 150, find the corresponding range of R_{out} and G_v.

7.87 An emitter follower, when driven from a 5-kΩ source, was found to have an output resistance R_{out} of 150 Ω. The output resistance increased to 250 Ω when the source resistance was increased to 10 kΩ. Find the overall voltage gain when the follower is driven by a 10-kΩ source and loaded by a 1-kΩ resistor.

7.88 For the general amplifier circuit shown in Fig. P7.88 neglect the Early effect.

(a) Find expressions for v_c/v_{sig} and v_e/v_{sig}.

(b) If v_{sig} is disconnected from node X, node X is grounded, and node Y is disconnected from ground and connected to v_{sig}, find the new expression for v_c/v_{sig}.

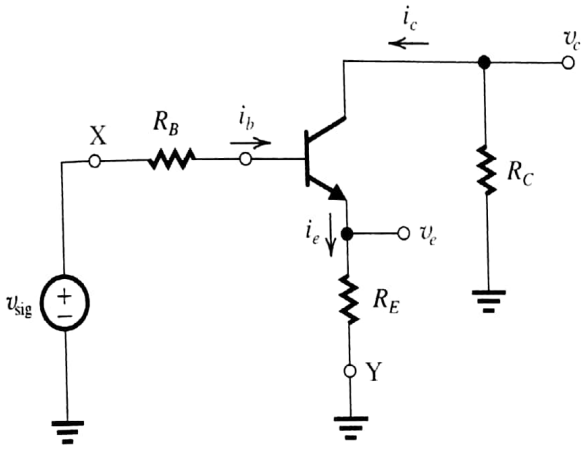

Figure P7.88

7.89 When the Early effect is neglected, the overall voltage gain of a CE amplifier with a collector resistance $R_C = 10\,\text{k}\Omega$ is calculated to be −100 V/V. If the BJT is biased at $I_C = 1$ mA and the Early voltage is 100 V, provide a better estimate of the voltage gain G_v.

***7.90** Show that when r_o is taken into account, the voltage gain of the source follower becomes

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_L \| r_o}{(R_L \| r_o) + \dfrac{1}{g_m}}$$

Now, with R_L removed, the voltage gain is carefully measured and found to be 0.98. Then, when R_L is connected and its value is varied, it is found that the gain is halved at $R_L = 500\ \Omega$. If the amplifier remained linear throughout this measurement, what must the values of g_m and r_o be?

D 7.91 In this problem, we investigate the effect of changing the bias current I_C on the overall voltage gain G_v of a CE amplifier. Consider the situation of a CE amplifier operating with a signal source having $R_{sig} = 10\,\text{k}\Omega$ and having $R_C \| R_L = 10\,\text{k}\Omega$. The BJT is specified to have $\beta = 100$ and $V_A = 25$ V. Use Eq. (7.114) (with r_o included in parallel with R_C and R_L in the numerator) to find $|G_v|$ at $I_C = 0.1$ mA, 0.2 mA, 0.5 mA, 1.0 mA, and 1.25 mA. Observe the effect of r_o on limiting $|G_v|$ as I_C is increased. Find the value of I_C that results in $|G_v| = 50$ V/V.

Section 7.4: Biasing

D 7.92 Consider the classical biasing scheme shown in Fig. 7.48(c), using a 9-V supply. For the MOSFET, $V_t = 1$ V, $\lambda = 0$, and $k_n = 2\ \text{mA/V}^2$. Arrange that the drain current is 1 mA, with about one-third of the supply voltage across each of R_S and R_D. Use 22 MΩ for the larger of R_{G1} and R_{G2}. What are the values of R_{G1}, R_{G2}, R_S, and R_D that you have chosen? Specify them to two significant digits. For your design, how far is the drain voltage from the edge of saturation?

D 7.93 Using the circuit topology displayed in Fig. 7.48(e), arrange to bias the NMOS transistor at $I_D = 0.5$ mA with V_D midway between cutoff and the beginning of triode operation. The available supplies are ±5 V. For the NMOS transistor, $V_t = 1.0$ V, $\lambda = 0$, and $k_n = 1\ \text{mA/V}^2$. Use a gate-bias resistor of 10 MΩ. Specify R_S and R_D to two significant digits.

D *7.94 In an electronic instrument using the biasing scheme shown in Fig. 7.48(c), a manufacturing error reduces R_S to zero. Let $V_{DD} = 15$ V, $R_{G1} = 10$ MΩ, and $R_{G2} = 5.1$ MΩ. What is the value of V_G created? If supplier specifications allow k_n to vary from 0.2 to 0.3 mA/V^2 and V_t to vary from 1.0 V to 1.5 V, what are the extreme values of I_D that may result? What value of R_S should have been installed to limit the maximum value of I_D to 1.5 mA? Choose an appropriate standard 5% resistor value (refer to Appendix J). What extreme values of current now result?

7.95 An NMOS transistor is connected in the bias circuit of Fig. 7.48(c), with $V_G = 5$ V and $R_S = 3\,\text{k}\Omega$. The transistor has $V_t = 1$ V and $k_n = 2\ \text{mA/V}^2$. What bias current results? If a transistor for which k_n is 50% higher is used, what is the resulting percentage increase in I_D?

SIM **7.96** The bias circuit of Fig. 7.48(c) is used in a design with $V_G = 5$ V and $R_S = 2\,\text{k}\Omega$. For a MOSFET with

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

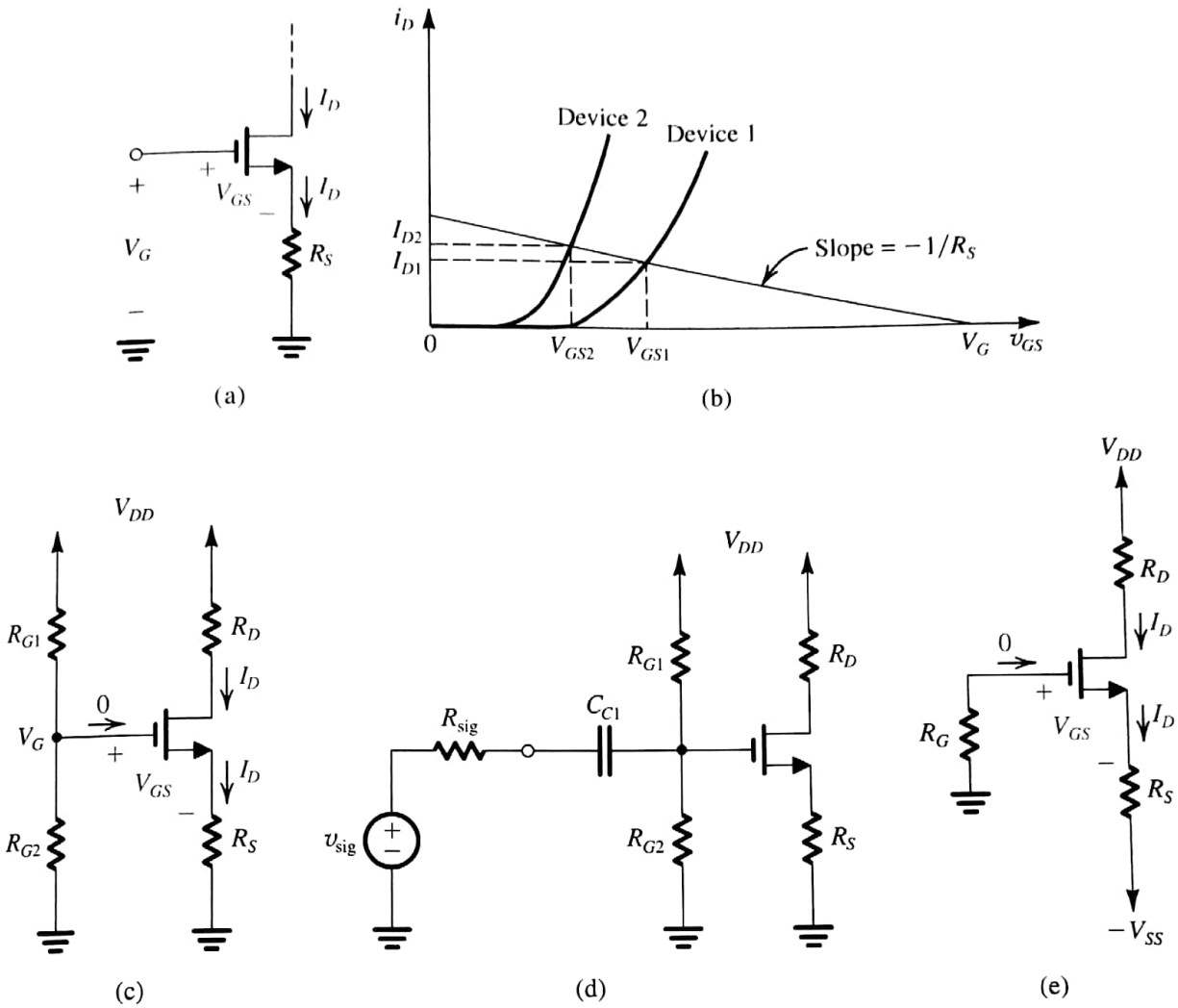

Figure 7.48 Biasing using a fixed voltage at the gate, V_G, and a resistance in the source lead, R_S: **(a)** basic arrangement; **(b)** reduced variability in I_D; **(c)** practical implementation using a single supply; **(d)** coupling of a signal source to the gate using a capacitor C_{C1}; **(e)** practical implementation using two supplies.

through a voltage divider (R_{G1}, R_{G2}). Since $I_G = 0$, R_{G1} and R_{G2} can be selected to be very large (in the megohm range), allowing the MOSFET to present a large input resistance to a signal source that may be connected to the gate through a coupling capacitor, as shown in Fig. 7.48(d). Here capacitor C_{C1} blocks dc and thus allows us to couple the signal v_{sig} to the amplifier input without disturbing the MOSFET dc bias point. The value of C_{C1} should be selected large enough to approximate a short circuit at all signal frequencies of interest. We shall study capacitively coupled MOSFET amplifiers, which are suitable only in discrete-circuit design, in Section 7.5. Finally, note that in the circuit of Fig. 7.48(c), resistor R_D is selected to be as large as possible to obtain high gain but small enough to allow for the desired signal swing at the drain while keeping the MOSFET in saturation at all times.

When two power supplies are available, as is often the case, the somewhat simpler bias arrangement of Fig. 7.48(e) can be utilized. This circuit is an implementation of Eq. (7.137), with V_G replaced by V_{SS}. Resistor R_G establishes a dc ground at the gate and presents a high input resistance to a signal source that may be connected to the gate through a coupling capacitor.

SIM **7.101** In the circuit of Fig. 7.50, let $R_G = 10\ \text{M}\Omega$, $R_D = 10\ \text{k}\Omega$, and $V_{DD} = 10\ \text{V}$. For each of the following two transistors, find the voltages V_D and V_G.

(a) $V_t = 1\ \text{V}$ and $k_n = 0.5\ \text{mA/V}^2$
(b) $V_t = 2\ \text{V}$ and $k_n = 1.25\ \text{mA/V}^2$

D 7.102 Using the feedback bias arrangement shown in Fig. 7.50 with a 5-V supply and an NMOS device for which $V_t = 1\ \text{V}$ and $k_n = 10\ \text{mA/V}^2$, find R_D to establish a drain current of 0.2 mA.

D 7.103 Figure P7.103 shows a variation of the feedback-bias circuit of Fig. 7.50. Using a 5-V supply with an NMOS transistor for which $V_t = 0.8\ \text{V}$, $k_n = 8\ \text{mA/V}^2$, and $\lambda = 0$, provide a design that biases the transistor at $I_D = 1\ \text{mA}$, with V_{DS} large enough to allow saturation operation for a 2-V negative signal swing at the drain. Use 22 MΩ as the largest resistor in the feedback-bias network. What values of R_D, R_{G1}, and R_{G2} have you chosen? Specify all resistors to two significant digits.

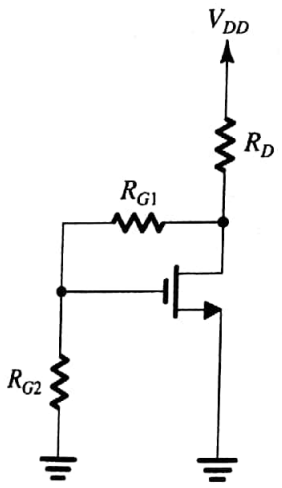

Figure P7.103

D 7.104 For the circuit in Fig. 7.51(a), neglect the base current I_B in comparison with the current in the voltage divider. It is required to bias the transistor at $I_C = 1\ \text{mA}$, which requires selecting R_{B1} and R_{B2} so that $V_{BE} = 0.710\ \text{V}$. If $V_{CC} = 3\ \text{V}$, what must the ratio R_{B1}/R_{B2} be? Now, if R_{B1} and R_{B2} are 1% resistors, that is, each can be in the range of 0.99 to 1.01 of its nominal value, what is the range obtained for V_{BE}? What is the corresponding range of I_C? If $R_C = 2\ \text{k}\Omega$, what is the range obtained for V_{CE}? Comment on the efficacy of this biasing arrangement.

D 7.105 It is required to bias the transistor in the circuit of Fig. 7.51(b) at $I_C = 1\ \text{mA}$. The transistor β is specified to be nominally 100, but it can fall in the range of 50 to 150. For $V_{CC} = +3\ \text{V}$ and $R_C = 2\ \text{k}\Omega$, find the required value of R_B to achieve $I_C = 1\ \text{mA}$ for the "nominal" transistor. What is the expected range for I_C and V_{CE}? Comment on the efficacy of this bias design.

D 7.106 Consider the single-supply bias network shown in Fig. 7.52(a). Provide a design using a 9-V supply in which the supply voltage is equally split between R_C, V_{CE}, and R_E with a collector current of 0.6 mA. The transistor β is specified to have a minimum value of 90. Use a voltage-divider current of $I_E/10$, or slightly higher. Since a reasonable design should operate for the best transistors for which β is very high, do your initial design with $\beta = \infty$. Then choose suitable 5% resistors (see Appendix J), making the choice in a way that will result in a V_{BB} that is slightly higher than the ideal value. Specify the values you have chosen for R_E, R_C, R_1, and R_2. Now, find V_B, V_E, V_C, and I_C for your final design using $\beta = 90$.

D 7.107 Repeat Problem 7.106, but use a voltage-divider current that is $I_E/2$. Check your design at $\beta = 90$. If you have the data available, find how low β can be while the value of I_C does not fall below that obtained with the design of Problem 7.106 for $\beta = 90$.

D *7.108 It is required to design the bias circuit of Fig. 7.52 for a BJT whose nominal $\beta = 100$.

(a) Find the largest ratio (R_B/R_E) that will guarantee I_E remains within ±5% of its nominal value for β as low as 50 and as high as 150.
(b) If the resistance ratio found in (a) is used, find an expression for the voltage $V_{BB} \equiv V_{CC}R_2/(R_1 + R_2)$ that will result in a voltage drop of $V_{CC}/3$ across R_E.
(c) For $V_{CC} = 5\ \text{V}$, find the required values of R_1, R_2, and R_E to obtain $I_E = 0.5\ \text{mA}$ and to satisfy the requirement for stability of I_E in (a).
(d) Find R_C so that $V_{CE} = 1.0\ \text{V}$ for β equal to its nominal value.

Check your design by evaluating the resulting range of I_E.

(g) What is the value of the dc base current I_B at the bias point? Assume $\beta = 100$. Characterize the signal current i_b that will be superimposed on the base current I_B.

(h) Dividing the amplitude of v_{be} by the amplitude of i_b, evaluate the incremental (or small-signal) input resistance of the amplifier.

(i) Sketch and clearly label correlated graphs for v_{BE}, v_{CE}, i_C, and i_B versus time. Note that each graph consists of a dc or average value and a superimposed sine wave. Be careful of the phase relationships of the sine waves.

7.20 The essence of transistor operation is that a change in v_{BE}, Δv_{BE}, produces a change in i_C, Δi_C. By keeping Δv_{BE} small, Δi_C is approximately linearly related to Δv_{BE}, $\Delta i_C = g_m \Delta v_{BE}$, where g_m is known as the transistor transconductance. By passing Δi_C through R_C, an output voltage signal Δv_O is obtained. Use the expression for the small-signal voltage gain in Eq. (7.20) to derive an expression for g_m. Find the value of g_m for a transistor biased at $I_C = 0.5$ mA.

7.21 The purpose of this problem is to illustrate the application of graphical analysis to the circuit shown in Fig. P7.21. Sketch $i_C - v_{CE}$ characteristic curves for the BJT for $i_B = 10\ \mu$A, 20 μA, 30 μA, and 40 μA. Assume the lines to be horizontal (i.e., neglect the Early effect), and let $\beta = 100$. For $V_{CC} = 5$ V and $R_C = 1$ kΩ, sketch the load line. What peak-to-peak collector voltage swing will result for i_B varying over the range 10 μA to 40 μA? If the BJT is biased at $V_{CE} = \frac{1}{2}V_{CC}$, find the value of I_C and I_B. If at this current $V_{BE} = 0.7$ V and if $R_B = 100$ kΩ, find the required value of V_{BB}.

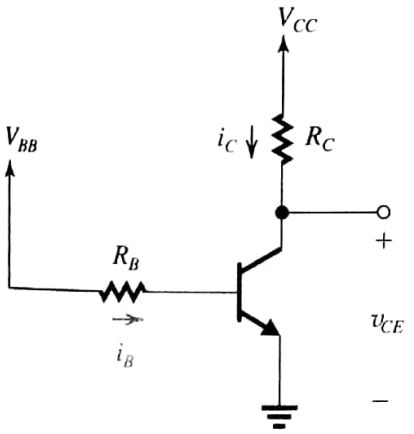

Figure P7.21

***7.22** Sketch the $i_C - v_{CE}$ characteristics of an *npn* transistor having $\beta = 100$ and $V_A = 100$ V. Sketch characteristic curves for $i_B = 20\ \mu$A, 50 μA, 80 μA, and 100 μA. For the purpose of this sketch, assume that $i_C = \beta i_B$ at $v_{CE} = 0$. Also, sketch the load line obtained for $V_{CC} = 10$ V and $R_C = 1$ kΩ. If the dc bias current into the base is 50 μA, write the equation for the corresponding $i_C - v_{CE}$ curve. Also, write the equation for the load line, and solve the two equations to obtain V_{CE} and I_C. If the input signal causes a sinusoidal signal of 30-μA peak amplitude to be superimposed on I_B, find the corresponding signal components of i_C and v_{CE}.

Section 7.2: Small-Signal Operation and Models

***7.23** This problem investigates the nonlinear distortion introduced by a MOSFET amplifier. Let the signal v_{gs} be a sine wave with amplitude V_{gs}, and substitute $v_{gs} = V_{gs} \sin \omega t$ in Eq. (7.28). Using the trigonometric identity $\sin^2\theta = \frac{1}{2} - \frac{1}{2}\cos 2\theta$, show that the ratio of the signal at frequency 2ω to that at frequency ω, expressed as a percentage (known as the second-harmonic distortion) is

$$\text{Second-harmonic distortion} = \frac{1}{4}\frac{V_{gs}}{V_{OV}} \times 100$$

If in a particular application V_{gs} is 10 mV, find the minimum overdrive voltage at which the transistor should be operated so that the second-harmonic distortion is kept to less than 1%.

7.24 Consider an NMOS transistor having $k_n = 10$ mA/V^2. Let the transistor be biased at $V_{OV} = 0.2$ V. For operation in saturation, what dc bias current I_D results? If a 0.02-V signal is superimposed on V_{GS}, find the corresponding increment in collector current by evaluating the total collector current i_D and subtracting the dc bias current I_D. Repeat for a –0.02-V signal. Use these results to estimate g_m of the FET at this bias point. Compare with the value of g_m obtained using Eq. (7.33).

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

The Signal Current in the Drain Terminal Next, consider the situation with the input signal v_{gs} applied. The total instantaneous gate-to-source voltage will be

$$v_{GS} = V_{GS} + v_{gs} \tag{7.27}$$

resulting in a total instantaneous drain current i_D,

$$\begin{aligned} i_D &= \frac{1}{2}k_n\left(V_{GS} + v_{gs} - V_t\right)^2 \\ &= \frac{1}{2}k_n(V_{GS} - V_t)^2 + k_n(V_{GS} - V_t)v_{gs} + \frac{1}{2}k_n v_{gs}^2 \end{aligned} \tag{7.28}$$

The first term on the right-hand side of Eq. (7.28) can be recognized as the dc bias current I_D (Eq. 7.25). The second term represents a current component that is directly proportional to the input signal v_{gs}. The third term is a current component that is proportional to the square of the input signal. This last component is undesirable because it represents *nonlinear distortion*. To reduce the nonlinear distortion introduced by the MOSFET, the input signal should be kept small so that

$$\frac{1}{2}k_n v_{gs}^2 \ll k_n(V_{GS} - V_t)v_{gs}$$

resulting in

$$v_{gs} \ll 2(V_{GS} - V_t) \tag{7.29}$$

or, equivalently,

$$v_{gs} \ll 2V_{OV} \tag{7.30}$$

If this **small-signal condition** is satisfied, we may neglect the last term in Eq. (7.28) and express i_D as

$$i_D \simeq I_D + i_d \tag{7.31}$$

where

$$i_d = k_n(V_{GS} - V_t)v_{gs}$$

The parameter that relates i_d and v_{gs} is the MOSFET **transconductance** g_m,

$$g_m \equiv \frac{i_d}{v_{gs}} = k_n(V_{GS} - V_t) \tag{7.32}$$

or in terms of the overdrive voltage V_{OV},

$$g_m = k_n V_{OV} \tag{7.33}$$

Figure 7.11 presents a graphical interpretation of the small-signal operation of the MOSFET amplifier. Note that g_m is equal to the slope of the i_D–v_{GS} characteristic at the bias point,

$$g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GS}} \tag{7.34}$$

This is the formal definition of g_m, which can be shown to yield the expressions given in Eqs. (7.32) and (7.33).

7.25 Consider the FET amplifier of Fig. 7.10 for the case $V_t = 0.4$ V, $k_n = 5$ mA/V^2, $V_{GS} = 0.6$ V, $V_{DD} = 1.8$ V, and $R_D = 10$ kΩ.

(a) Find the dc quantities I_D and V_{DS}.
(b) Calculate the value of g_m at the bias point.
(c) Calculate the value of the voltage gain.
(d) If the MOSFET has $\lambda = 0.1$ V^{-1}, find r_o at the bias point and calculate the voltage gain.

D *7.26 An NMOS amplifier is to be designed to provide a 0.20-V peak output signal across a 20-kΩ load that can be used as a drain resistor. If a gain of at least 10 V/V is needed, what g_m is required? Using a dc supply of 1.8 V, what values of I_D and V_{OV} would you choose? What W/L ratio is required if $\mu_n C_{ox} = 200\ \mu$A/V^2? If $V_t = 0.4$ V, find V_{GS}.

D *7.27 In this problem we investigate an optimum design of the CS amplifier circuit of Fig. 7.10. First, use the voltage gain expression $A_v = -g_m R_D$ together with Eq. (7.42) for g_m to show that

$$A_v = -\frac{2I_D R_D}{V_{OV}} = -\frac{2(V_{DD} - V_{DS})}{V_{OV}}$$

Next, let the maximum positive input signal be $\hat{v}_i$. To keep the second-harmonic distortion to an acceptable level, we bias the MOSFET to operate at an overdrive voltage $V_{OV} \gg \hat{v}_i$. Let $V_{OV} = m\hat{v}_i$. Now, to maximize the voltage gain $|A_v|$, we design for the lowest possible V_{DS}. Show that the minimum V_{DS} that is consistent with allowing a negative signal voltage swing at the drain of $|A_v|\ \hat{v}_i$ while maintaining saturation-mode operation is given by

$$V_{DS} = \frac{V_{OV} + \hat{v}_i + 2V_{DD}(\hat{v}_i/V_{OV})}{1 + 2(\hat{v}_i/V_{OV})}$$

Now, find V_{OV}, V_{DS}, A_v, and $\hat{v}_o$ for the case $V_{DD} = 2.5$ V, $\hat{v}_i = 20$ mV, and $m = 15$. If it is desired to operate this transistor at $I_D = 200\ \mu$A, find the values of R_D and W/L, assuming that for this process technology $k'_n = 100\ \mu$A/V^2.

7.28 In the table below, for MOS transistors operating under a variety of conditions, complete as many entries as possible. Although some data is not available, it is always possible to calculate g_m using one of Eqs. (7.40), (7.41), or (7.42). Assume $\mu_n = 500$ cm^2/V·s, $\mu_p = 250$ cm^2/V·s, and $C_{ox} = 0.4$ fF/μm^2.

		Voltages (V)				Dimensions (μm)				
Case	Type	I_D (mA)	$\lvert V_{GS}\rvert$	$\lvert V_t\rvert$	V_{OV}	W	L	W/L	$k'(W/L)$	g_m(mA/V)
a	N	1	3	2			1			
b	N	1		0.7	0.5	50				
c	N	10			2		1			
d	N	0.5			0.5					
e	N	0.1				10	2			
f	N		1.8	0.8		40	4			
g	P	0.5						25		
h	P		3	1					0.5	
i	P	10				4000	2			
j	P	10			4					
k	P				1	30	3			
l	P				5				0.08	

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

7.29 An NMOS technology has $\mu_n C_{ox} = 250\ \mu A/V^2$ and $V_t = 0.5$ V. For a transistor with $L = 0.5\ \mu m$, find the value of W that results in $g_m = 2$ mA/V at $I_D = 0.25$ mA. Also, find the required V_{GS}.

7.30 For the NMOS amplifier in Fig. P7.30, replace the transistor with its T equivalent circuit, assuming $\lambda = 0$. Derive expressions for the voltage gains v_s/v_i and v_d/v_i.

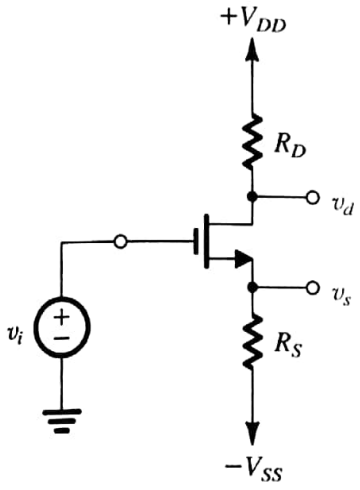

Figure P7.30

SIM **7.31** In the circuit of Fig. P7.31, the NMOS transistor has $|V_t| = 0.5$ V and $V_A = 50$ V and operates with $V_D = 1$ V. What is the voltage gain v_o/v_i ? What do V_D and the gain become for I increased to 1 mA?

7.32 For a 0.18-μm CMOS fabrication process: $V_{tn} = 0.5$ V, $V_{tp} = -0.5$ V, $\mu_n C_{ox} = 400\ \mu A/V^2$, $\mu_p C_{ox} = 100\ \mu A/V^2$, $C_{ox} = 8.6$ fF/μm^2, V_A (n-channel devices) $= 5L$ (μm), and $|V_A|$ (p-channel devices) $= 6L$ (μm). Find the small-signal model parameters (g_m and r_o) for both an NMOS and a PMOS transistor having $W/L = 10\ \mu m/0.5\ \mu m$ and operating at $I_D = 100\ \mu A$. Also, find the overdrive voltage at which each device must be operating.

***7.33** Figure P7.33 shows a discrete-circuit amplifier. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite). All capacitors behave as short circuits for signals and as open circuits for dc.

(a) If the transistor has $V_t = 1$ V, and $k_n = 4$ mA/V^2, verify that the bias circuit establishes $V_{GS} = 1.5$ V, $I_D = 0.5$ mA, and $V_D = +7.0$ V. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.

(b) Find g_m and r_o if $V_A = 100$ V.

(c) Draw a complete small-signal equivalent circuit for the amplifier, assuming all capacitors behave as short circuits at signal frequencies.

(d) Find R_{in}, v_{gs}/v_{sig}, v_o/v_{gs}, and v_o/v_{sig}.

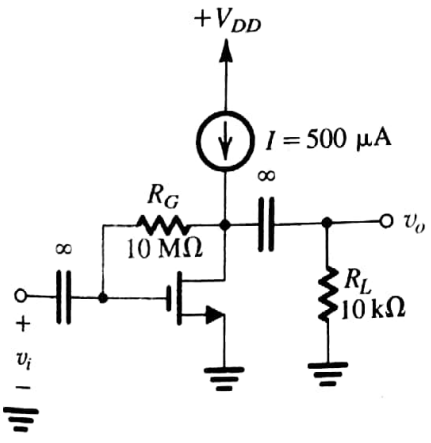

Figure P7.31

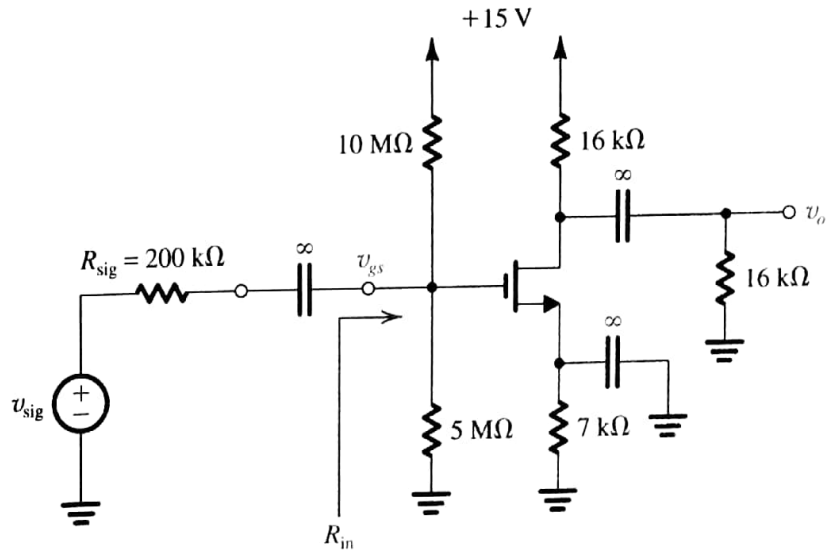

Figure P7.33

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem