

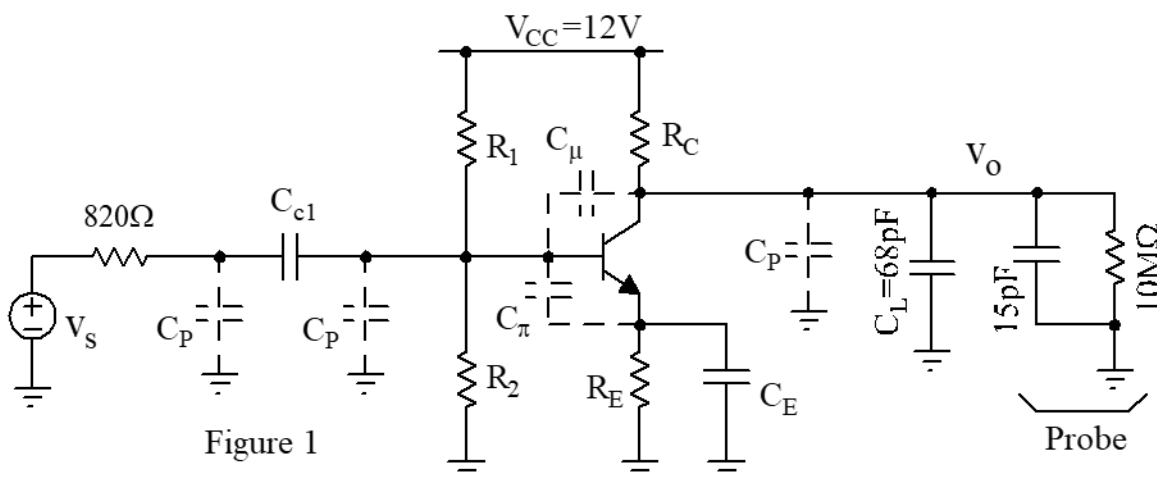
Laboratory 5: Common Emitter Amplifier Design Project

Issued Tuesday, Oct. 9, 2018 \Rightarrow Due 5 p.m., Tuesday, Nov. 6, 2018

A. OBJECTIVE

In this laboratory exercise, you will design, build, and demonstrate a one-stage common emitter amplifier that meets the following specifications:

- (a) Midband gain: $A_v = \left| \frac{v_o}{v_s} \right| > 160 \text{ V/V}$
- (b) Lower corner frequency: $f_l < 100 \text{ Hz}$
- (c) Upper corner frequency: $f_h > 160 \text{ kHz}$
- (d) Rise time: $t_r < 4 \text{ } \mu\text{sec}$
- (e) Undistorted output voltage swing: $V_o(\text{max}) > 1.5 V_{\text{zero-to-peak}}$
- (f) All specifications must be met while loaded by an oscilloscope probe and a load capacitor $C_L=68\text{pF}$.
- (g) Minimize total external capacitance (coupling and bypass).
- (h) Reasonable bias stability: $\frac{R_E}{\alpha} \geq 10 \frac{R_B}{\beta}$, $V_B \geq 2.5 \text{ V}$
- (i) All resistors and capacitors must be standard 10% values (no parallel/series combination).
- (j) $R_s = 820\Omega$, $R_c < 100\text{k}\Omega$.
- (k) Circuit topology depicted in Fig. 1
- (l) Use transistor 2N3904. (See data sheets in your course packs.)



Note that there is no output coupling capacitor in Fig. 1. This lab has three phases: hand design, SPICE simulation, and lab verification. You must write a complete laboratory report describing your efforts in a professional-looking format, e.g., with figure captions, tables, etc.