EE 105 | Discussion 2

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Discussion Outline

- Overview of SPICE
 - What is SPICE?
 - SPICE Workflow
 - Netlist Syntax
 - Topology & Analysis
 - Running a SPICE Simulation
 - Viewing Simulation Results
 - Beyond the Basics
- Opamp practice



What is SPICE?

Simulation

Program with

ntegrated

Circuit

Emphasis

- Software used for analog circuit simulation (originally intended for developing ICs)
 - Developed @ UC Berkeley—version 1 released in 1973 (under public domain)
- Started out as a command-line tool
- Now multiple companies offer their own packaged versions of spice
 - LTspice, HSPICE, PSpice



SPICE Workflow





What is a Netlist?

- A simple text file that contains a *circuit description* and *analysis options*
- Different circuit elements specified by unique letters
- Circuit topology is defined by:
 - giving each node a unique name
 - assigning elements between these nodes



Netlist Syntax

- Filename ends in .sp
 - L.g., mycircuit.sp
- First line is always a comment!
- Not case sensitive
 - vs = Vs = VS = vS
- Last line must be .end
- Other than first/last line, order doesn't matter

```
1 EE105 SPICE Tutorial Example 1 - Simple RC Circuit
2 vs vs gnd PWL(Os OV 5ms OV 5.001ms 5V 10ms 5V)
3 r1 vs vo 1k
4 c1 vo gnd 1uF
5 .tran 0.01ms 10ms
6 .option post=2 nomod
7 .end
```



Netlist Syntax | Topology

- Each line denotes a different circuit element
 - The 1st character defines the type of element and the following characters denote the name of the element
 - The 2nd term is the first node the element is connected to
 - The 3rd term is the second node the element is connected to (more nodes will follow for devices with >2 terminals)
 - The last term is the element value/properties (can use prefixes f, p, n, u, m, k, meg, giga & tera to denote magnitude)

```
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```



Netlist Syntax | Topology

- Circuit nodes & elements can have the same name
- gnd is a standard name for global ground (can also use 0)
- Order of nodes matters for things like sources!

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Netlist Syntax | Topology

• What does this circuit look like? Draw using labels that match the netlist.

1 EE105 SPICE Tutorial Example 1 - Simple RC Circuit 2 vs vs gnd PWL(0s 0V 5ms 0V 5.001ms 5V 10ms 5V) 3 r1 vs vo 1k 4 c1 vo gnd 1uF 5 .tran 0.01ms 10ms 6 .option post=2 nomod 7 .end



Netlist Syntax | Analysis

- Line 5 tells HSPICE to perform a transient analysis from time t = 0 ms to t = 10 ms in steps of 10 μ s
- Line 6 tells HSPICE to generate waveform files necessary for viewing in *awaves* while not including model info in the output

```
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5 .tran 0.01ms 10ms
6 .option post=2 nomod
7 .end
```



Simulating in HSPICE

• To simulate the circuit, simply run the command below in a UNIX terminal

hspice mycircuit.sp > mycircuit.lis

- This will run the simulation and store the outputs in mycircuit.lis
- You can open mycircuit.lis and check for errors/operating points, but most of the time we'll be interested in looking at plots of voltages and currents



Viewing Simulation Results

 To run *awaves*, use the command below (make sure you have X11 enabled!)

awaves &

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- This will run the *awaves* software and leave your terminal free to use
- Click "Open Waveform File"
 & navigate to the file called mycircuit.tr0

Search CustomExplorer Console		—		×
File Edit Tools Options Windows Help			SYNO	PSYS
Import a New Design				
Open Existing Design(s)				
Open Waveform File	paya, inc.			
Load Session	Version J-2014.09 8 Aug 22 2014 11:04:31			
Save Session	21:31 (PID:14578)			
Run Tcl Script				
Save Log As				
Exit				_
Log History				
Command				M



Viewing Simulation Results

• This will open up the Custom WaveView window, where you can add traces to view





Beyond the Basics

- Can perform many different type of analyses
 - AC (.ac), DC (.dc), transfer function (.tf), DC operating point (.op)
- For nonlinear devices (diodes, MOSFETs), must define a model to specify device parameters
 - Model names cannot start w/ a number!

```
1 EE105 SPICE Tutorial Example 2 - Simple Diode Circuit
2 .model tut_diode d (is=1e-14 vj=0.6 rs=10)
3 vs vs gnd 5V
4 rs vs vd 5k
5 d1 vd gnd tut_diode
6 .op
7 .end
```



Ideal Opamps

- Find an expression for v_{o1} and v_{o2}:
- Two key properties of ideal opamps:
 - Infinite input resistance
 - Infinite gain
- Follow the currents





Ideal Opamps

• $i_1 = v_s/R_1$

- $v_{o1} = -(R_2 + R_3)i_1 = -v_s(R_2 + R_3)/R_1$
- $v_{o2} = -(R_2)i_1 = -v_s(R_2/R_1)$



