EE 105 | Discussion 4

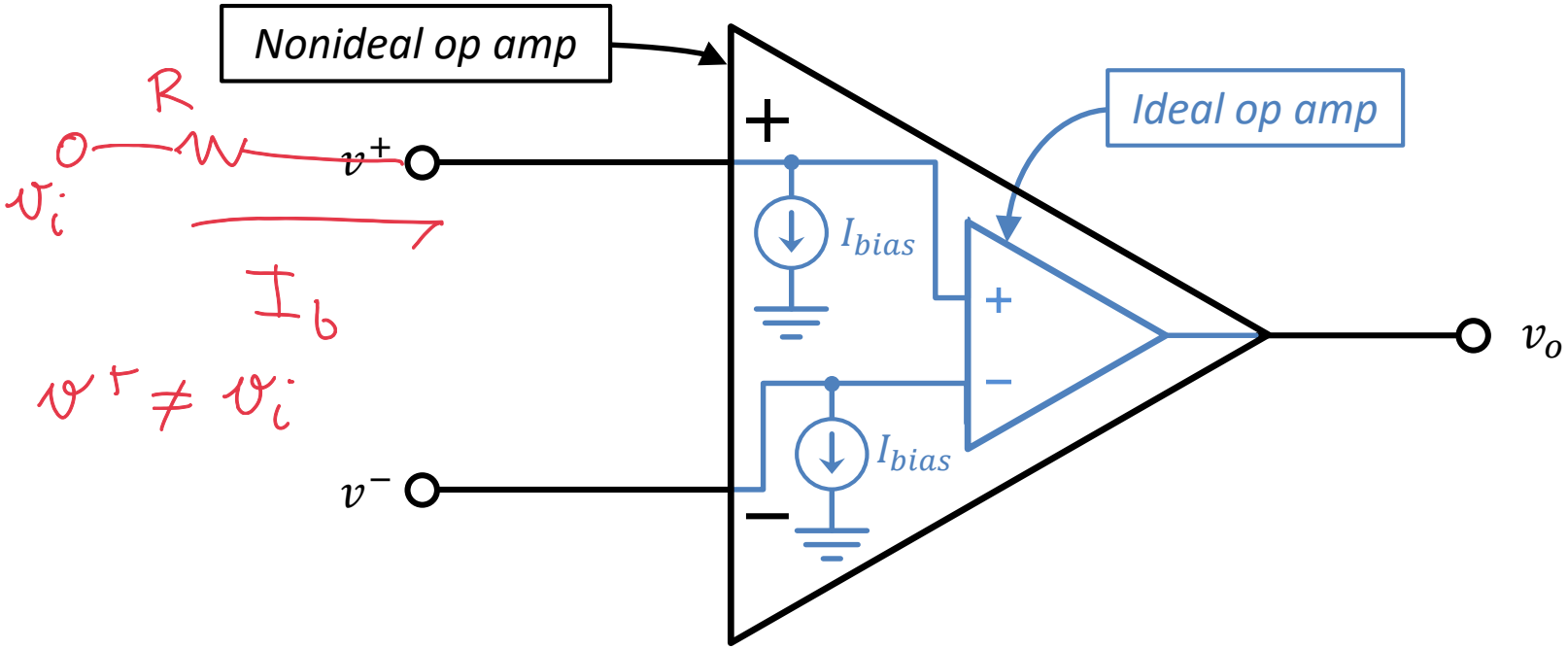
Ali Ameri & Kieran Peleaux

Discussion Outline

- Offset current (i.e., what happens when we have different input bias currents on each input?)
- Design constraints

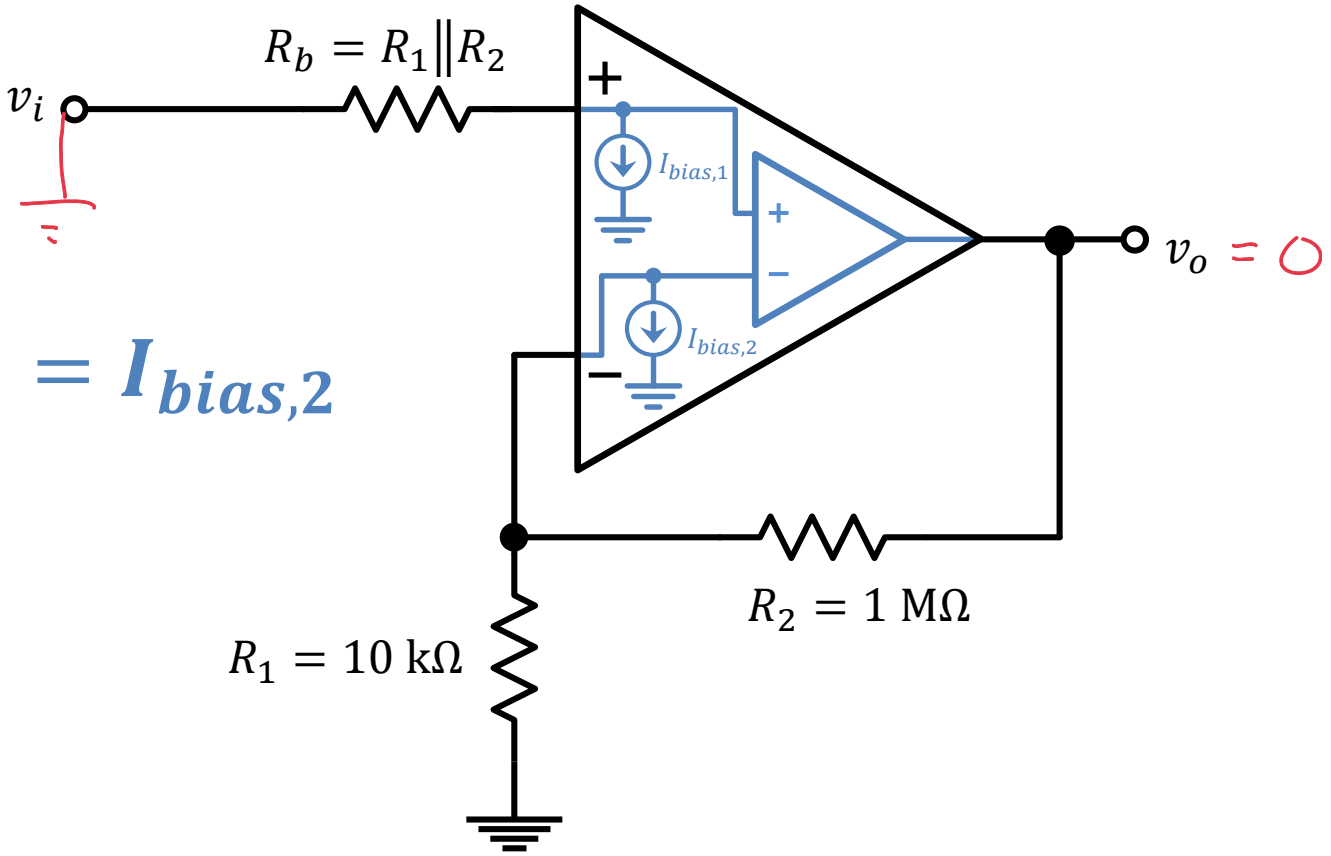
Nonideal Op Amps | Input Bias Current

Remember the model for input bias current



Nonideal Op Amps | Bias Current Compensation

Last week, we found out we could compensate for this bias current—*this only works if the currents are matched*!

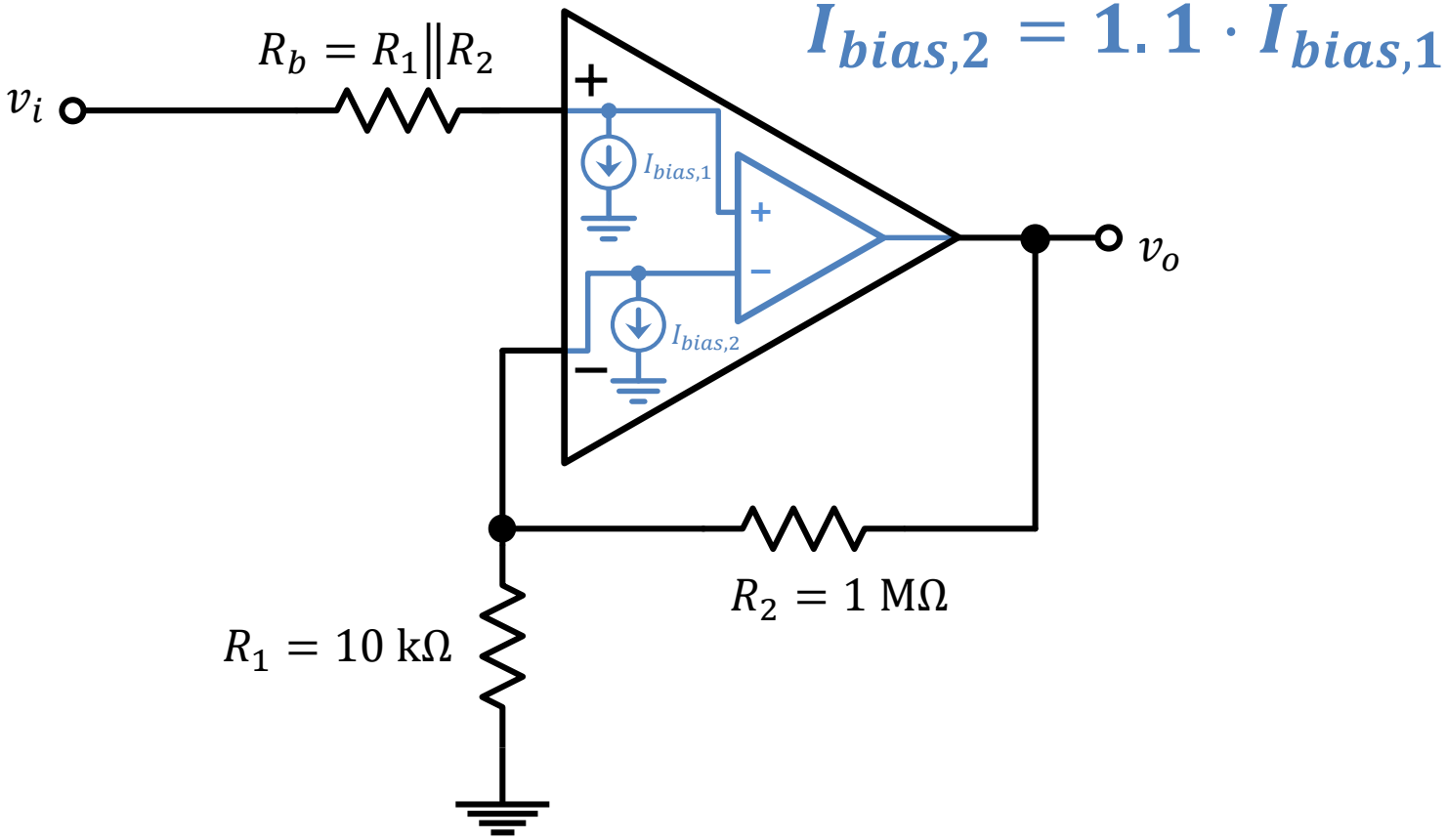


$$I_{bias,1} = I_{bias,2}$$

Nonideal Op Amps | Offset Current

Now, consider an offset current that is 10% of $I_{bias,1}$
→ What's the resulting v_o (ignoring any V_{OS})?

$I_{bias,1} = 200\,nA$

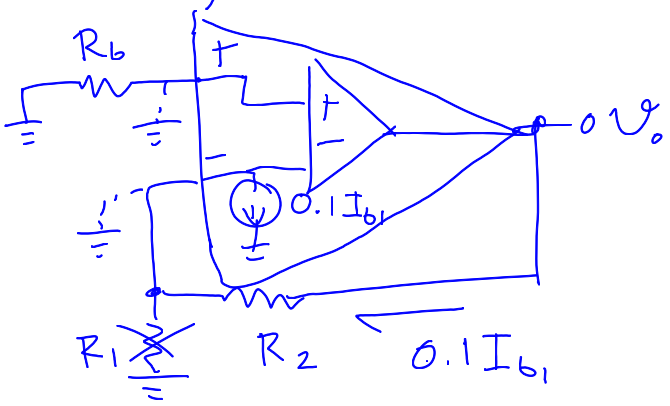


Nonideal Op Amps | Current Offset

Now, consider an offset current that is 10% of I_{bias}
→ What's the resulting v_o (ignoring any V_{OS})?

Using superposition:

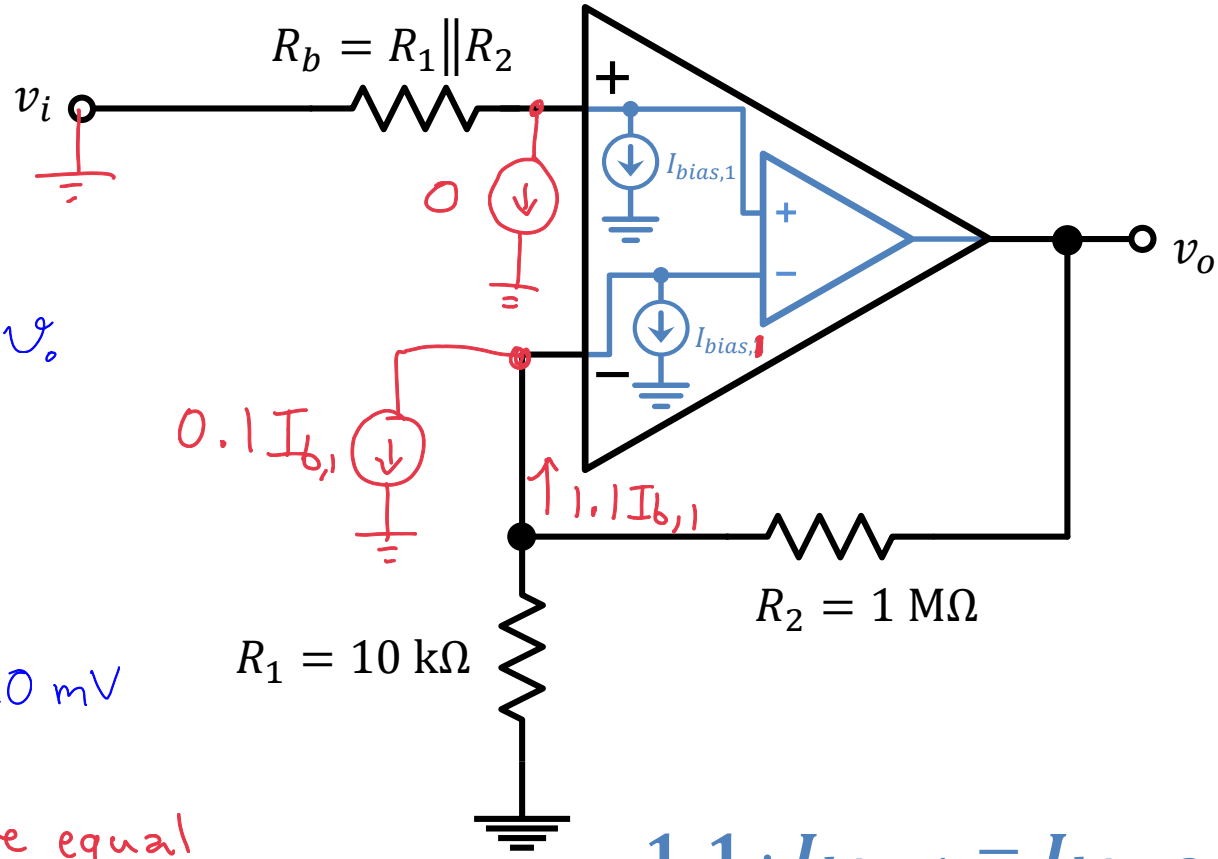
① OC $I_{b,1}$ sources



$v_o = v^- + (0.1I_{b1})R_2 = 20\text{ mV}$

② OC red I sources

↳ input bias currents are equal
w/ R_b → $v_o = 0$



$1.1 \cdot I_{bias,1} = I_{bias,2}$

$v_{o,total} = 20\text{mV} + 0 = 20\text{mV}$

Nonideal Op Amps | Voltage & Current Offsets

Now include previous $V_{OS} = 2\,mV$ & $I_{OS} = 0.1 \cdot I_{bias}$ to find the ***worst-case*** dc voltage at the output in this compensated circuit

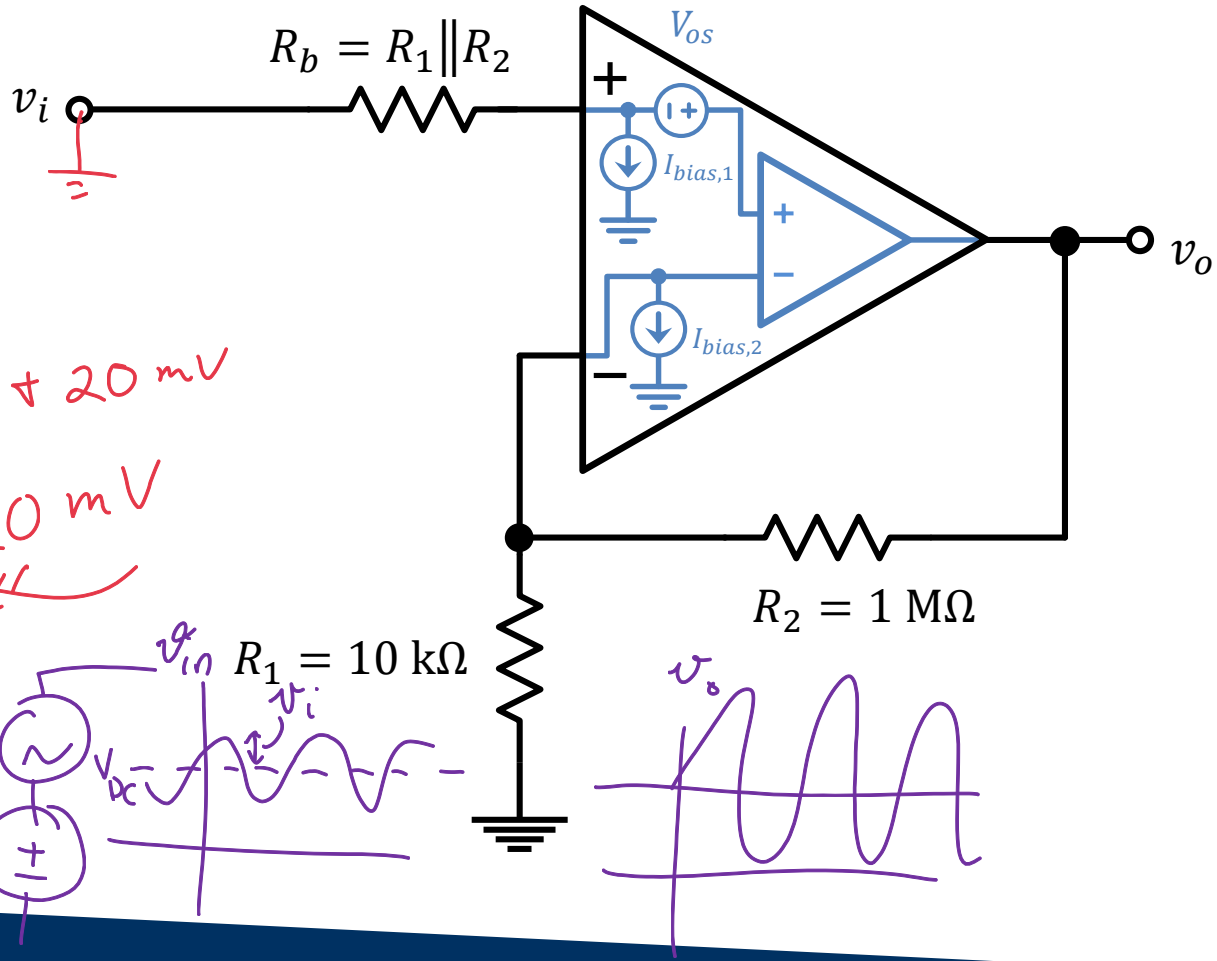
From last week:

if $V_{os} = 2$ mV

↳ $v_o = 200$ mV

worst-case $v_o = 200 + 20$ mV

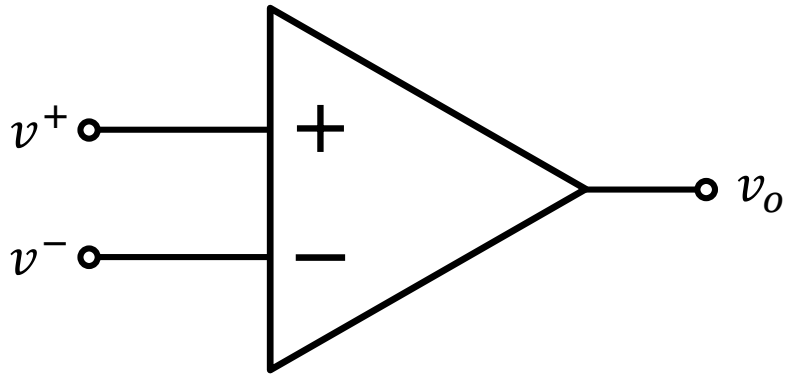
$= 220$ mV



Constrained Op Amp Design

Let's look at how you might be constrained by a COTS (commercial off-the-shelf) part when trying to design a circuit

- $f_t = 20\ MHz$
- Slew rate, SR $= 10\,\frac{V}{\mu s}$
- Output saturation, $V_{o,max} = 10\ V$



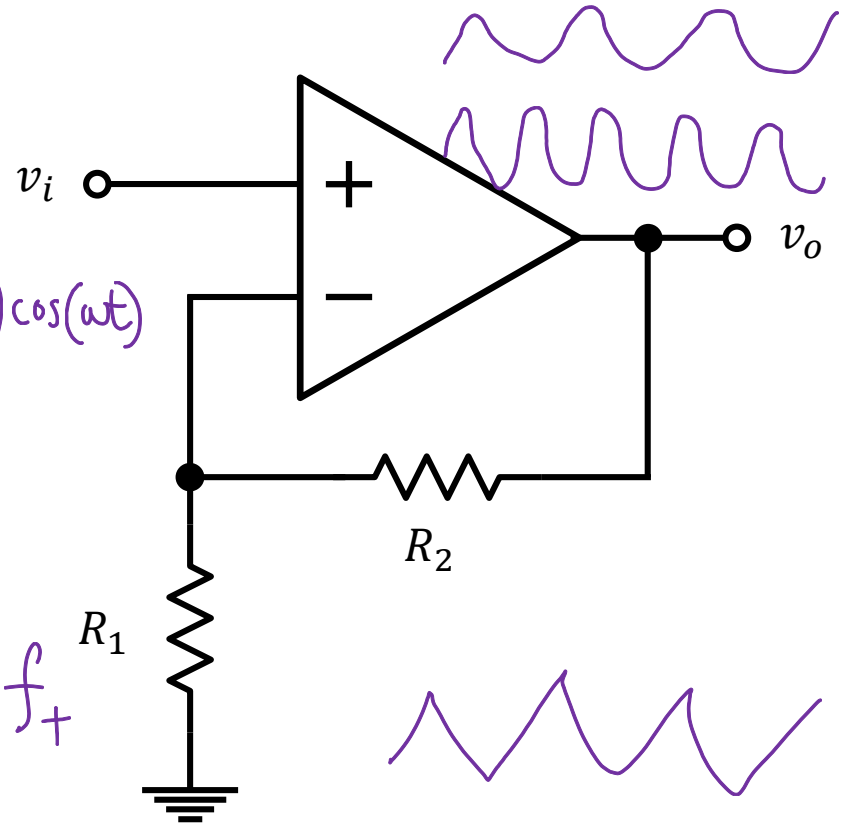
Constrained Op Amp Design

Using the noninverting configuration with

- $A_v = 10\frac{\text{V}}{\text{V}}$
- $v_i = 0.5\ \text{V}$ → $v_o = 5\ \text{V}$

- ☐ $f_t = 20\ MHz$ $v_o(t) = (5\text{V})\sin(\omega t)$
- ☑ $\text{SR} = 10\frac{V}{\mu s}$
- ☒ ☐ $V_{o,max} = 10\ V$

What's the maximum frequency signal that can be amplified before output distortion occurs?



$$SR \geq \frac{dv_o(t)}{dt} = \omega v_o \cos(\omega t) = \omega (A_v v_i)\cos(\omega t)$$

$$\left.\frac{dv_o(t)}{dt}\right|_{max} = \omega_{max} A_v v_i = 10\ V/\mu s$$

$$\omega_{max} = 2\times10^6\ \text{rad/sec}$$

$$f_{max} = 318\ \text{kHz} << f_t$$

Constrained Op Amp Design

Using the noninverting configuration with

- $f = 200\ \text{kHz} \ll f_t$

What's the maximum input signal amplitude that can be amplified before output distortion occurs?

- ☒ $f_t = 20\ MHz$
- ☑ $\text{SR} = 10\ \frac{V}{\mu s}$
- ☒ $V_{o,max} = 10\ V$

$\downarrow$

$V_{i,max} = 1\ V$

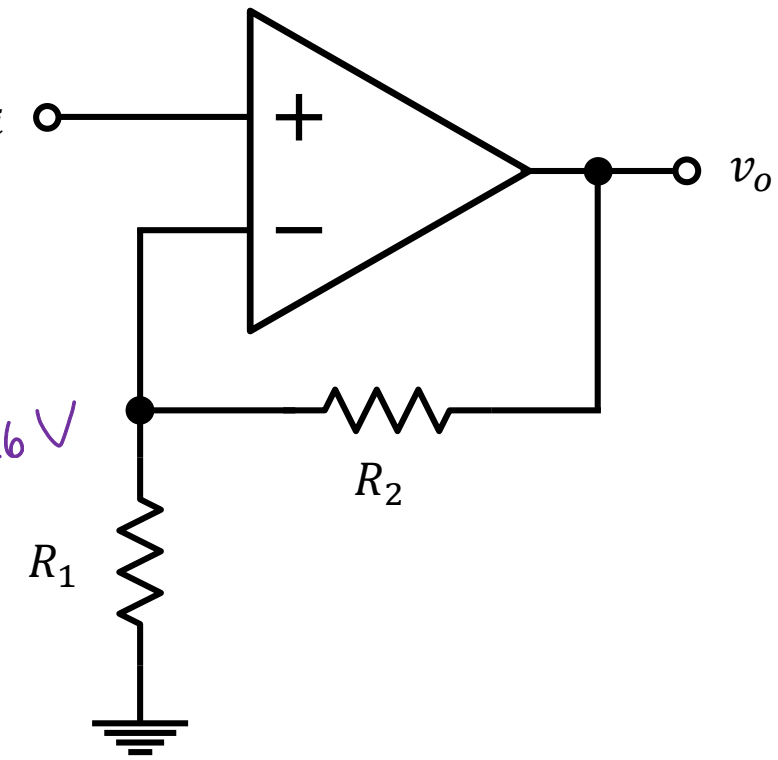
$\text{SR} = (2\pi f)(A_v v_i)$, with $v_o = A_v v_i$

$\frac{10\ V}{\mu s} = (2\pi \cdot 200\text{kHz})(10 v_i)$

$v_i = 796\ \text{mV}$

$\Rightarrow v_o = (10)(796\ \text{mV}) = 7.96\ \text{V}$

$v_o < V_{o,max}$



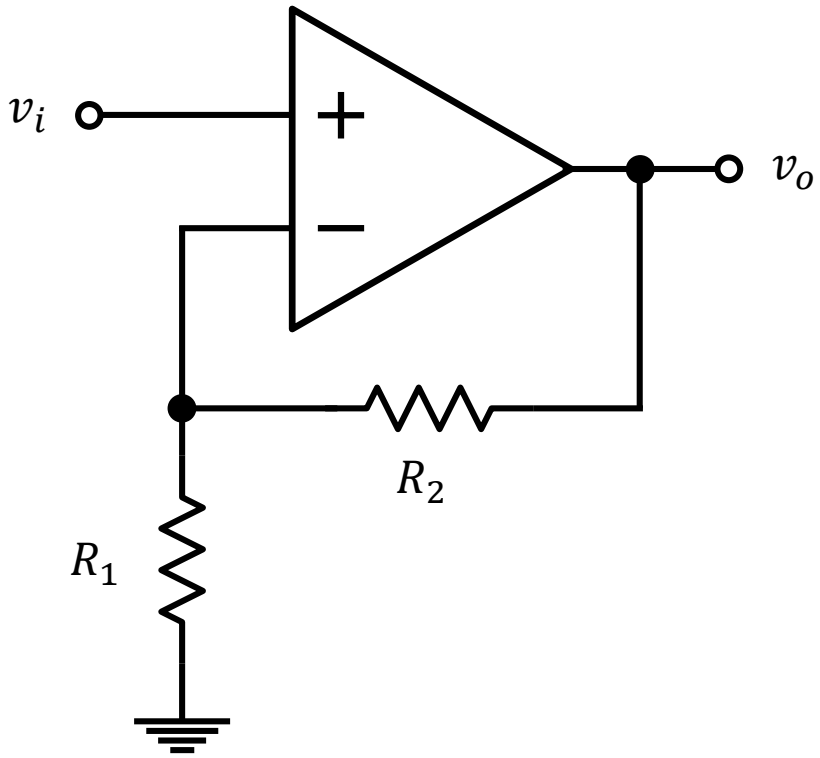
Constrained Op Amp Design

Using the noninverting configuration with

- $v_i = 50\ \text{mV} \rightarrow v_o = 0.5\ V$

- ☑ $f_t = 20\ MHz$
- ☒ ☑ $\text{SR} = 10\ \frac{V}{\mu s}$
- ☒ ☑ $V_{o,max} = 10\ V$

What's the useable frequency range?



(1) $f_T = GBW = A_V f_{3dB}$

$$f_{3dB} = \frac{f_T}{A_V} = 2\ MHz$$

$$10\frac{V}{\mu s} = (2\pi f)(A_V v_i)$$

$$f = \frac{(10 \times 10^6\ V/s)}{2\pi \cdot 0.5V} = 3.18\ MHz$$

Constrained Op Amp Design

Using the noninverting configuration with

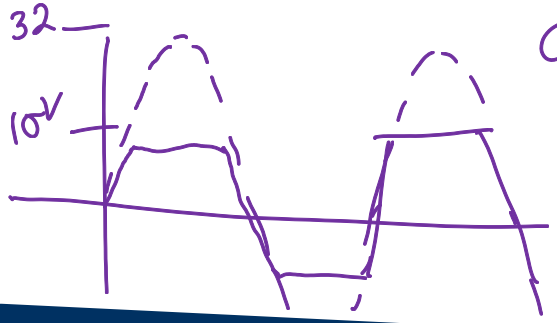
- $f = 50\ kHz$

What's the useable input voltage range?

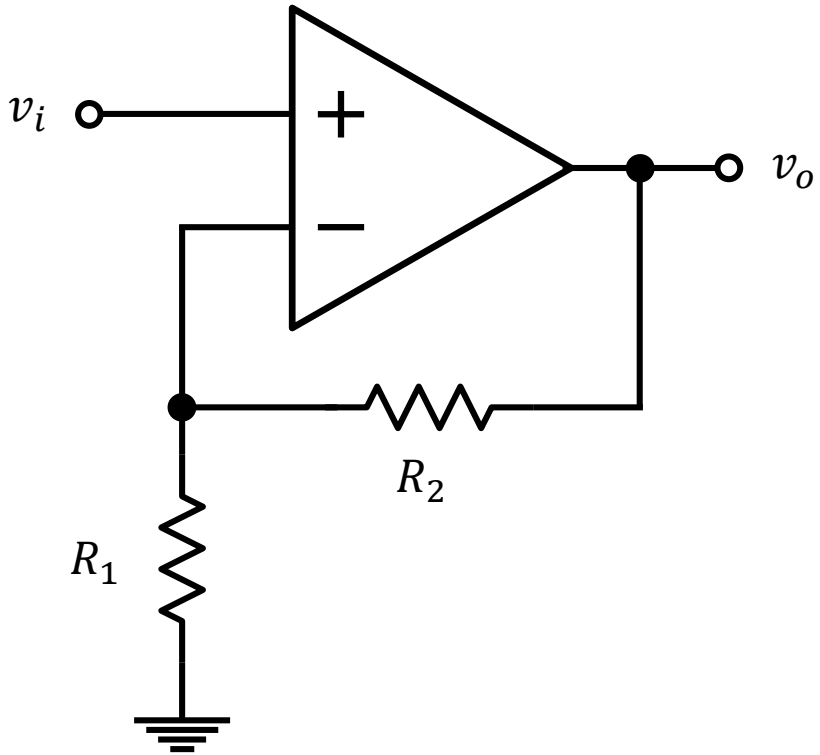
- ☒ $f_t = 20\ MHz \rightarrow f_{3dB} = 2MHz > f$
- ☒ SR $= 10 \frac{V}{\mu s}$
- ☑ $V_{o,max} = 10\ V$

$$10 \frac{V}{\mu s} = (2\pi \cdot 50kHz)(10 \cdot v_{i,max})$$

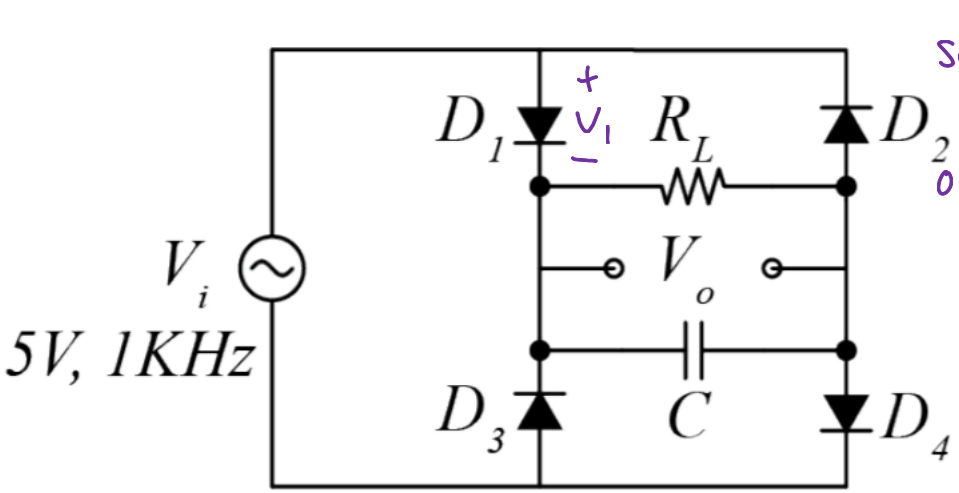
$$v_{i,max} = 3.18^V \rightarrow v_o = 31.8^V$$



$0V < v_i < 1V$



Homework 2, SPICE Diode circuit



SC: D_1 ON when $V_1 > 0.7V$

OC: D_1 OFF otherwise

Example SPICE file

```
TA Version of Homework 2 SPICE Problem
*$
vs vi gnd sin(0 5 1kHz)
d1 vi vop D1N4148
d2 vi von D1N4148
d3 gnd vop D1N4148
d4 gnd von D1N4148
rl vop von 1kOhm
cl vop von 1uF
.tran 1us 5ms
.model D1N4148  D(Is=5.84n N=1.94 Rs=.7017 Ikf=44.17m Xti=3 Eg=1.11
 Cjo=.95p M=.55 Vj=.75 Fc=.5 Isr=11.07n Nr=2.088 Bv=100 Ibv=100u Tt
=11.07n)
.options post=2 nomod
.end
```

Homework 2, SPICE Diode circuit

Simulation Output