D 8.67 Design the CMOS cascode amplifier in Fig. 8.33 for the following specifications: $g_{m1} = 1$ mA/V and $A_v = -280$ V/V. Assume that for the available fabrication process, $|V_A'| = 5$ V/μm for both NMOS and PMOS devices and that $\mu_n C_{ox} = 4\,\mu_p C_{ox} = 400$ μA/V^2. Use the same channel length L for all devices and operate all four devices at $|V_{OV}| = 0.25$ V. Determine the required channel length L, the bias current I, and the W/L ratio for each of four transistors. Assume that suitable bias voltages have been chosen, and neglect the Early effect in determining the W/L ratios.

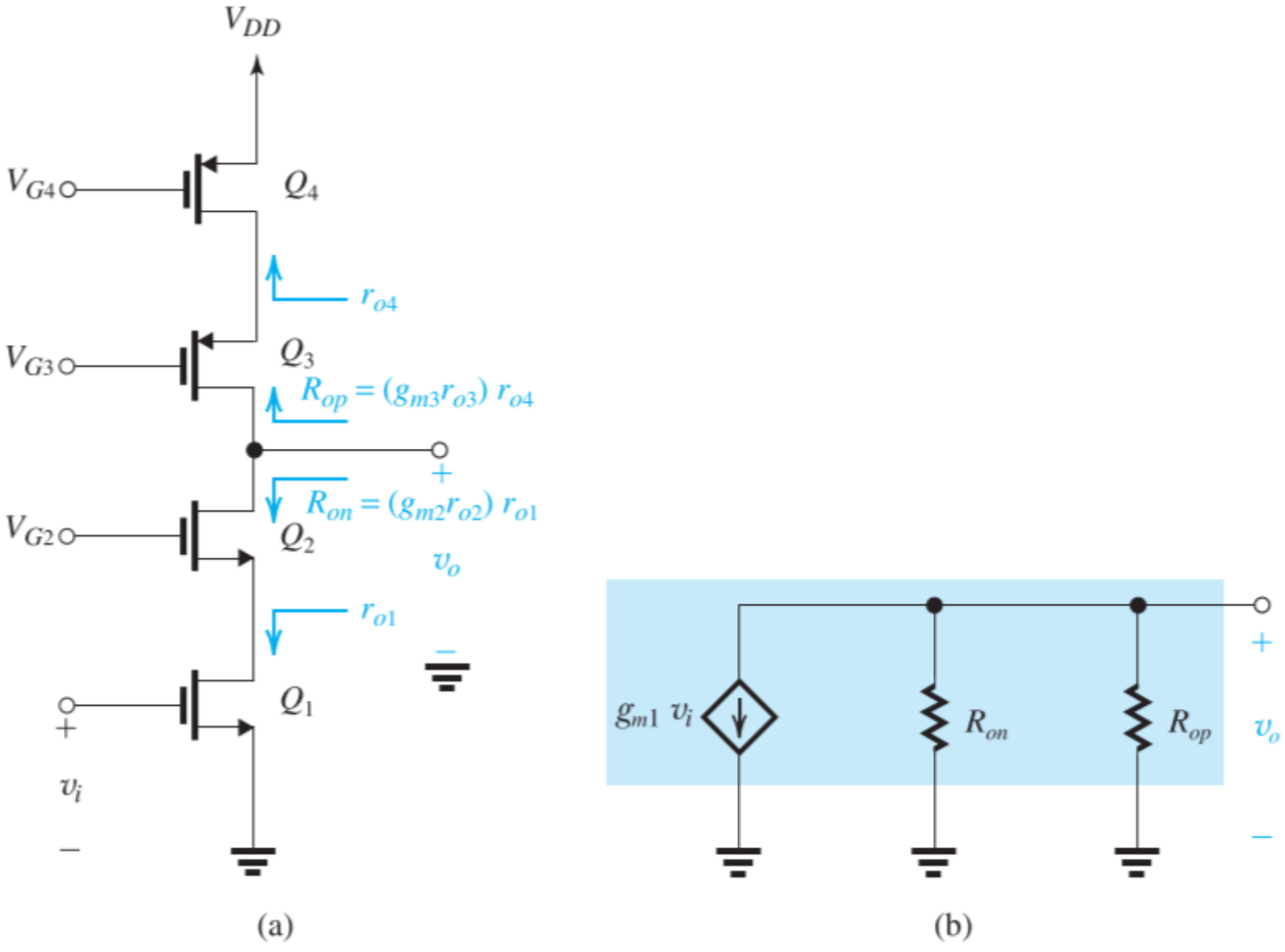

Figure 8.33 A cascode amplifier with a cascode current-source load.

10.76 Consider a bipolar cascode amplifier biased at a current of 1 mA. The transistors used have $\beta = 100$, $r_o = 100\ \text{k}\Omega$, $C_\pi = 10\ \text{pF}$, $C_\mu = 2\ \text{pF}$, $C_{cs} = 0$, and $r_x = 50\ \Omega$. The amplifier is fed with a signal source having $R_{\text{sig}} = 5\ \text{k}\Omega$. The load resistance $R_L = 2\ \text{k}\Omega$. Find the low-frequency gain A_M, and estimate the value of the 3-dB frequency f_H.

14.18 For a particular inverter design using a power supply V_{DD}, $V_{OL} = 0.1V_{DD}$, $V_{OH} = 0.8V_{DD}$, $V_{IL} = 0.4V_{DD}$, and $V_{IH} = 0.6\,V_{DD}$. What are the noise margins? What is the width of the transition region? For a minimum noise margin of 0.4 V, what value of V_{DD} is required?

16.43 Consider a ring oscillator consisting of five inverters, each having $t_{PLH} = 3\ \text{ns}$ and $t_{PHL} = 2\ \text{ns}$. Sketch one of the output waveforms, and specify its frequency and the percentage of the cycle during which the output is high.