PROBLEM SET #11

Issued: Monday, November 25, 2019

Due: Tuesday, December 10, 2019, at 12:00 noon via Gradescope.

1. Sedra & Smith, Problem 8.67
2. Sedra & Smith, Problem 10.76
3. For Problem 3, consider the differential amplifier show in Fig. PS11.1 below.
   (a) What are the Q-points $[I_D, V_{DS}]$ for the transistors in the amplifier given the parameters in table PS11.1 below? Find the differential-mode gain A_{dm} $\left(\frac{v_{od}}{v_{id}}\right)$, common-mode gain A_{cm} $\left(\frac{v_{ocm}}{v_{icm}}\right)$, CMRR (common-mode rejection ratio, $\left|\frac{A_{dm}}{A_{cm}}\right|$), and differential-mode and common-mode input resistances.

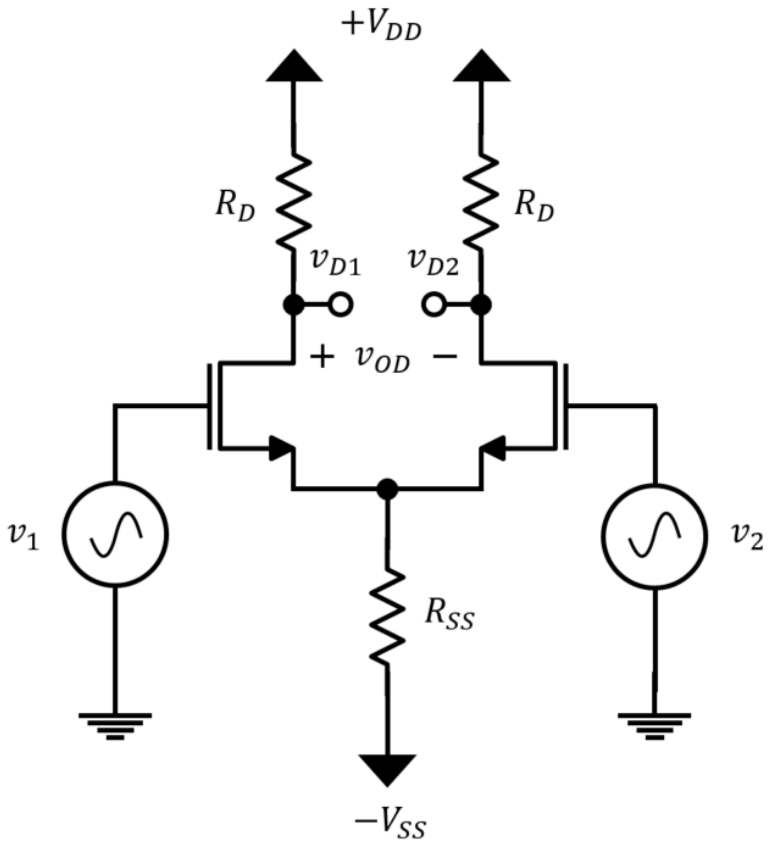

Figure PS11.1

PARAMETER	*VALUE*	*UNIT*
k_n	500	μA/V^2
V_{tn}	1.1	V
V_{DD}	12	V
V_{SS}	12	V
R_{SS}	200	kΩ
R_D	10	kΩ

Table PS11.1

(b) Show that, for the differential amplifier in Fig. PS11.1, if there exists a mismatch between drain resistances, ΔR_D and between transconductances, Δg_m, then the common-mode gain is given by

$$A_{cm} \approx \left(\frac{R_D}{2R_{ss}}\right) \cdot \left(\frac{\Delta g_m}{g_m} + \frac{\Delta R_D}{R_D}\right)$$

(c) If the common-mode gain is measured to be 0.5 mV/V, what is the percentage change in R_D (i.e. $\frac{\Delta R_D}{R_D} \times 100$) required in one of the two drain resistors so as to reduce A_{cm} to zero?

4. What is the propagation delay for a minimum-size CMOS inverter with the parameters given in Table PS11.2 in which both *W/L* ratios are 2/1? What are the approximate the rise and fall times of the inverter? Assume a load capacitance of 0.25 pF and $V_{DD} = 5$ V.

5. What are the sizes of the transistors in the CMOS inverter with the parameters given in Table PS11.2 if it must drive a 0.5 pF capacitance with an average propagation delay of 5 ns? Design the inverter for equal rise and fall times. Assume $V_{DD} = 5$ V.

6. Design a symmetrical CMOS reference inverter to provide a delay of 1 ns when driving a 10-pF load for (a) $V_{DD} = 5$ V and (b) $V_{DD} = 3.3$ V. Assume $V_{tn} = -V_{tp} = 0.7$ V.

7. Sedra & Smith, Problem 14.18

8. What are the noise margins for a symmetrical CMOS inverter operating with $V_{DD} = 5$ V and $V_{tn} = -V_{tp} = 0.75$ V?

9. What are the noise margins of a minimum size CMOS inverter in which both *W/L* ratios are 2/1, the transistors have the parameters given in Table PS11.2, and $V_{DD} = 3.3$ V?

PARAMETER	***VALUE***	***UNIT***
k_n'	50	μA/V^2
k_p'	20	μA/V^2
V_{tn}	1	V
V_{tp}	-1	V

Table PS11.2

10. One method to estimate the average propagation delay of an inverter is to construct a long chain of inverters, connected as a ring as shown in Figure PS11.2. This circuit is called a *ring oscillator*, and the output of any inverter in the chain will be similar to a square wave.

(a) Suppose that the chain contains 143 inverters and the average propagation delay of an inverter is 120 ps. What will the frequency of the square wave generated by the oscillator be?

(b) Why should the number of inverters be odd? What could happen if an even number of inverters were used in the ring oscillator?

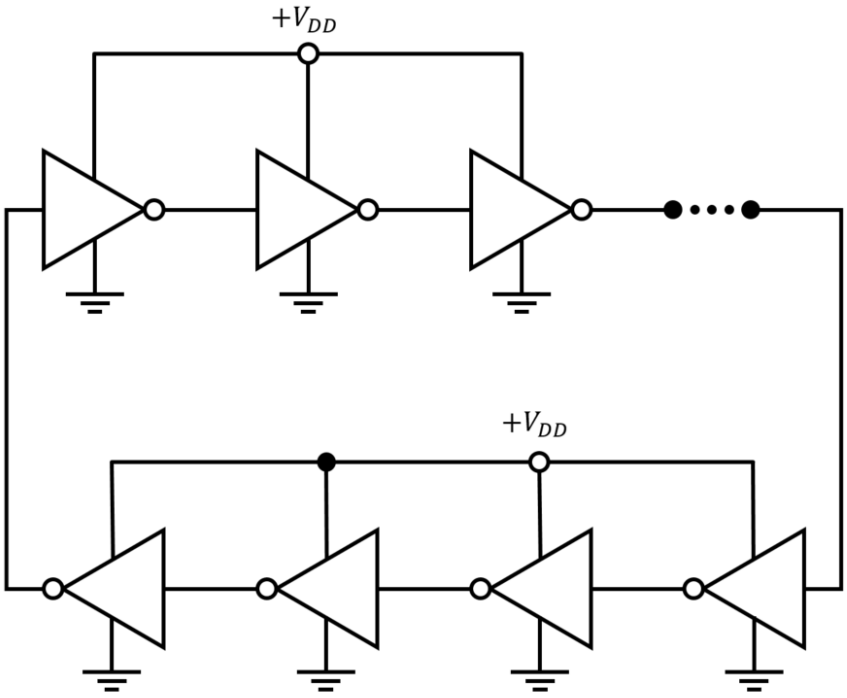

Figure PS10.2

11. Sedra & Smith, Problem 16.43