**3.25** For a particular junction for which $C_{j0} = 0.4$ pF, $V_0 = 0.75$ V, and $m = 1/3$, find $C_j$ at reverse-bias voltages of 1 V and 10 V.

**3.26** The junction capacitance $C_j$ can be thought of as that of a parallel-plate capacitor and thus given by

$$C_j = \frac{\epsilon A}{W}$$

Show that this approach leads to a formula identical to that obtained by combining Eqs. (3.43) and (3.45) [or equivalently, by combining Eqs. (3.47) and (3.48)].

$$\alpha = A\sqrt{2\epsilon_s q \frac{N_A N_D}{N_A + N_D}} \qquad (3.43)$$

This incremental-capacitance approach turns out to be quite useful in electronic circuit design, as we shall see throughout this book.

Using Eq. (3.44) together with Eq. (3.42) yields

$$C_j = \frac{\alpha}{2\sqrt{V_0 + V_R}} \qquad (3.45)$$

The value of $C_j$ at zero reverse bias can be obtained from Eq. (3.45) as

$$C_{j0} = \frac{\alpha}{2\sqrt{V_0}} \qquad (3.46)$$

which enables us to express $C_j$ as

$$C_j = \frac{C_{j0}}{\sqrt{1 + \dfrac{V_R}{V_0}}} \qquad (3.47)$$

where $C_{j0}$ is given by Eq. (3.46) or alternatively if we substitute for $\alpha$ from Eq. (3.43) by

$$C_{j0} = A\sqrt{\left(\frac{\epsilon_s q}{2}\right)\left(\frac{N_A N_D}{N_A + N_D}\right)\left(\frac{1}{V_0}\right)} \qquad (3.48)$$

**D 4.37** Assuming the availability of diodes for which $v_D = 0.75$ V at $i_D = 1$ mA, design a circuit that utilizes four diodes connected in series, in series with a resistor $R$ connected to a 15-V power supply. The voltage across the string of diodes is to be 3.3 V.

**4.43** For the circuits in Fig. P4.9, using the constant-voltage-drop $(V_D = 0.7$ V) diode model, find the values of the labeled currents and voltages.
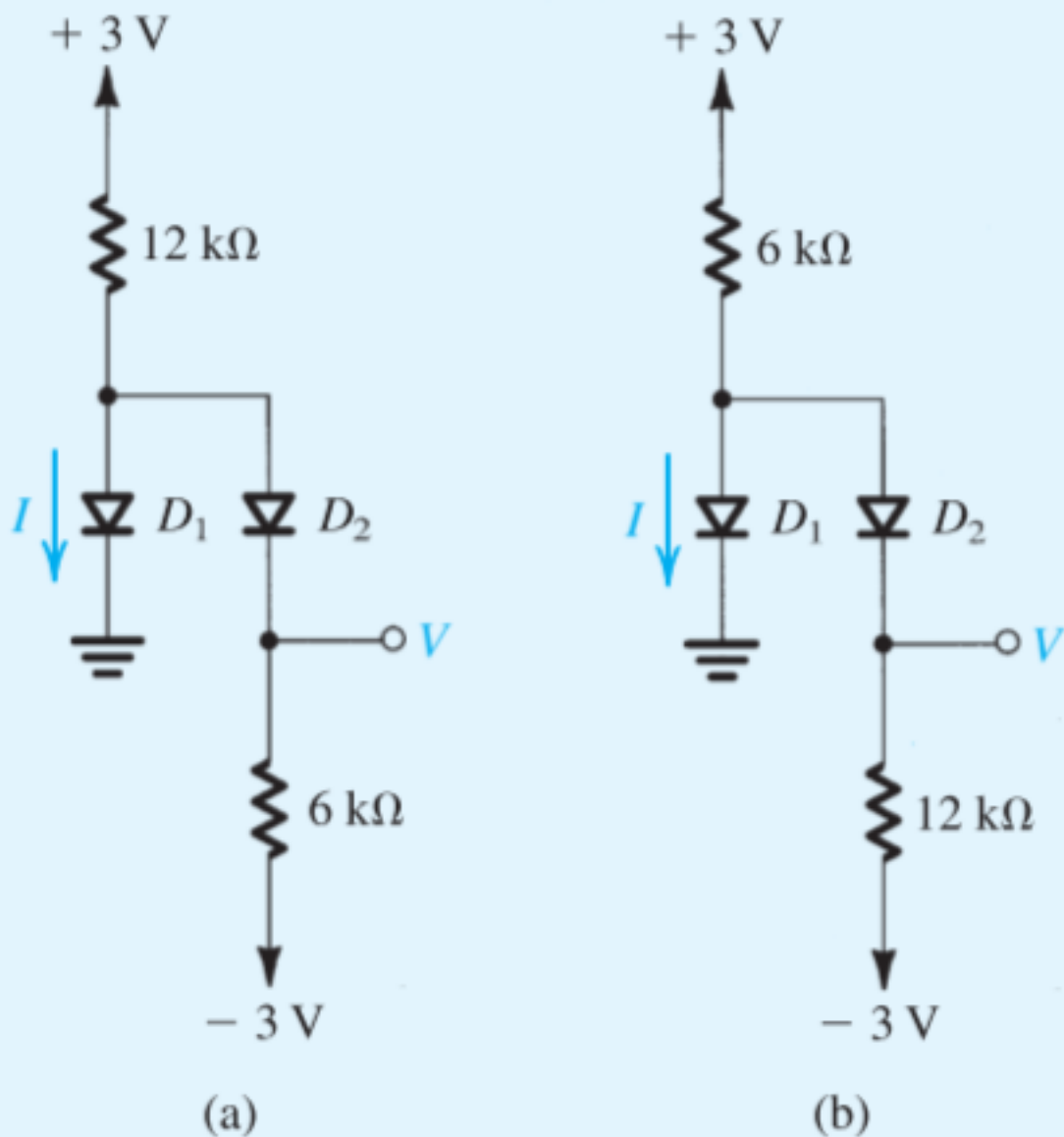


**Figure P4.9**

**5.23** An NMOS transistor, fabricated with $W = 20\,\mu\text{m}$ and $L = 1\,\mu\text{m}$ in a technology for which $k'_n = 100\,\mu\text{A/V}^2$ and $V_t = 0.8\,\text{V}$, is to be operated at very low values of $v_{DS}$ as a linear resistor. For $v_{GS}$ varying from 1.0 V to 4.8 V, what range of resistor values can be obtained? What is the available range if

(a) the device width is halved?
(b) the device length is halved?
(c) both the width and length are halved?

| Case | Voltage (V) | | | | | | Region of operation |
|------|------|------|------|------|------|------|------|
| | $V_S$ | $V_G$ | $V_D$ | $V_{GS}$ | $V_{OV}$ | $V_{DS}$ | |
| a | +1.0 | +1.0 | +2.0 | | | | |
| b | +1.0 | +2.5 | +2.0 | | | | |
| c | +1.0 | +2.5 | +1.5 | | | | |
| d | +1.0 | +1.5 | 0 | | | | |
| e | 0 | +2.5 | +1.0 | | | | |
| f | +1.0 | +1.0 | +1.0 | | | | |
| g | −1.0 | 0 | 0 | | | | |
| h | −1.5 | 0 | 0 | | | | |
| i | −1.0 | 0 | +1.0 | | | | |
| j | +0.5 | +2.0 | +0.5 | | | | |

**\*5.27** The table above lists 10 different cases labeled (a) to (j) for operating an NMOS transistor with $V_t = 1\,\text{V}$. In each case the voltages at the source, gate, and drain (relative to the circuit ground) are specified. You are required to complete the table entries. Note that if you encounter a case for which $v_{DS}$ is negative, you should exchange the drain and source before solving the problem. You can do this because the MOSFET is a symmetric device.

**5.24** When the drain and gate of a MOSFET are connected together, a two-terminal device known as a "diode-connected transistor" results. Figure P5.24 shows such devices obtained from MOS transistors of both polarities. Show that

(a) the $i$–$v$ relationship is given by

$$i = \frac{1}{2}k'\frac{W}{L}(v - |V_t|)^2$$

(b) the incremental resistance $r$ for a device biased to operate at $v = |V_t| + V_{OV}$ is given by

$$r \equiv 1\Big/\left[\frac{\partial i}{\partial v}\right] = 1\Big/\left(k'\frac{W}{L}V_{OV}\right)$$



(a)                                    (b)

**Figure P5.24**