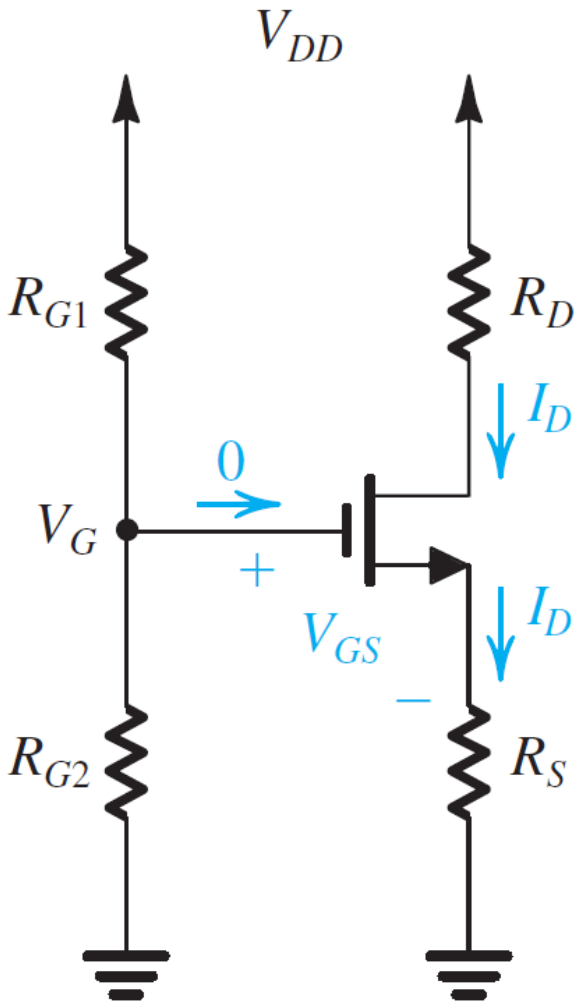
D 7.92 Consider the classical biasing scheme shown in Fig. 7.48(c), using a 9-V supply. For the MOSFET, $V_t = 1$ V, $\lambda = 0$, and $k_n = 2$ mA/V^2. Arrange that the drain current is 1 mA, with about one-third of the supply voltage across each of R_S and R_D. Use 22 MΩ for the larger of R_{G1} and R_{G2}. What are the values of R_{G1}, R_{G2}, R_S, and R_D that you have chosen? Specify them to two significant digits. For your design, how far is the drain voltage from the edge of saturation?



(c)

Figure 7.48 Biasing using a fixed

D ***7.94** In an electronic instrument using the biasing scheme shown in Fig. 7.48(c), a manufacturing error reduces R_S to zero. Let $V_{DD} = 15$ V, $R_{G1} = 10$ MΩ, and $R_{G2} = 5.1$ MΩ. What is the value of V_G created? If supplier specifications allow k_n to vary from 0.2 to 0.3 mA/V^2 and V_t to vary from 1.0 V to 1.5 V, what are the extreme values of I_D that may result? What value of R_S should have been installed to limit the maximum value of I_D to 1.5 mA? Choose an appropriate standard 5% resistor value (refer to Appendix J). What extreme values of current now result?

D ***7.108** It is required to design the bias circuit of Fig. 7.52 for a BJT whose nominal $\beta = 100$.

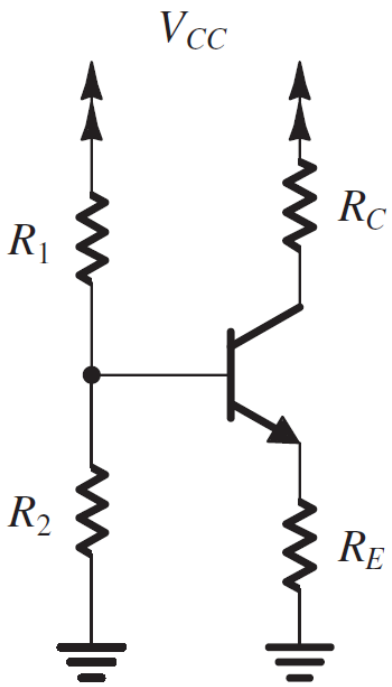
(a) Find the largest ratio (R_B/R_E) that will guarantee I_E remains within ±5% of its nominal value for β as low as 50 and as high as 150.

(b) If the resistance ratio found in (a) is used, find an expression for the voltage $V_{BB} \equiv V_{CC}R_2/(R_1 + R_2)$ that will result in a voltage drop of $V_{CC}/3$ across R_E.

(c) For $V_{CC} = 5$ V, find the required values of R_1, R_2, and R_E to obtain $I_E = 0.5$ mA and to satisfy the requirement for stability of I_E in (a).

(d) Find R_C so that $V_{CE} = 1.0$ V for β equal to its nominal value.

Check your design by evaluating the resulting range of I_E.



(a)

Figure 7.52 Classical biasing for BJTs

7.24 Consider an NMOS transistor having $k_n = 10\ \text{mA/V}^2$. Let the transistor be biased at $V_{OV} = 0.2$ V. For operation in saturation, what dc bias current I_D results? If a 0.02-V signal is superimposed on V_{GS}, find the corresponding increment in collector current by evaluating the total collector current i_D and subtracting the dc bias current I_D. Repeat for a –0.02-V signal. Use these results to estimate g_m of the FET at this bias point. Compare with the value of g_m obtained using Eq. (7.33).

***7.33** Figure P7.33 shows a discrete-circuit amplifier. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite). All capacitors behave as short circuits for signals and as open circuits for dc.

(a) If the transistor has $V_t = 1$ V, and $k_n = 4$ mA/V^2, verify that the bias circuit establishes $V_{GS} = 1.5$ V, $I_D = 0.5$ mA, and $V_D = +7.0$ V. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.

(b) Find g_m and r_o if $V_A = 100$ V.

(c) Draw a complete small-signal equivalent circuit for the amplifier, assuming all capacitors behave as short circuits at signal frequencies.

(d) Find R_{in}, v_{gs}/v_{sig}, v_o/v_{gs}, and v_o/v_{sig}.

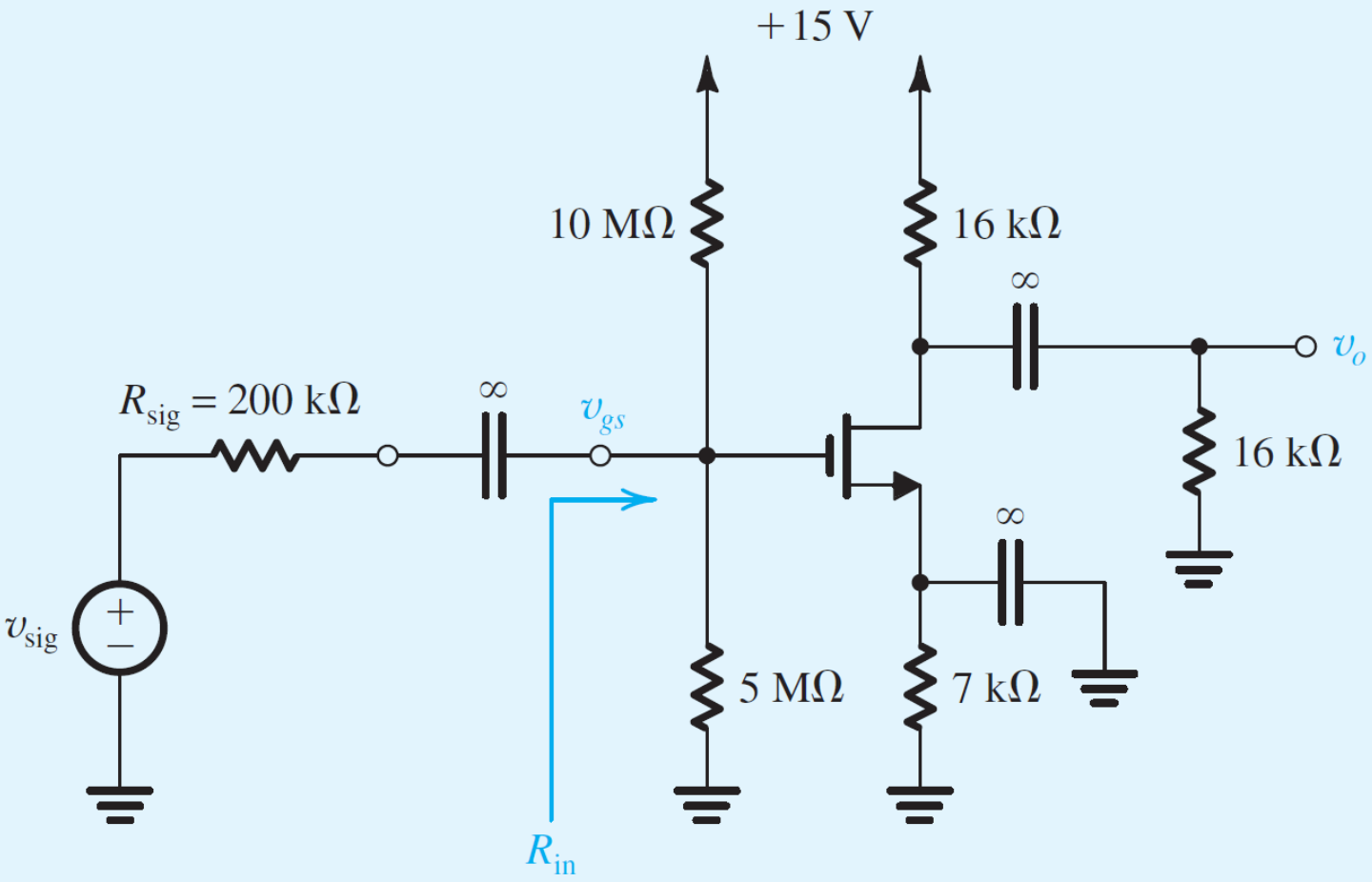


Figure P7.33