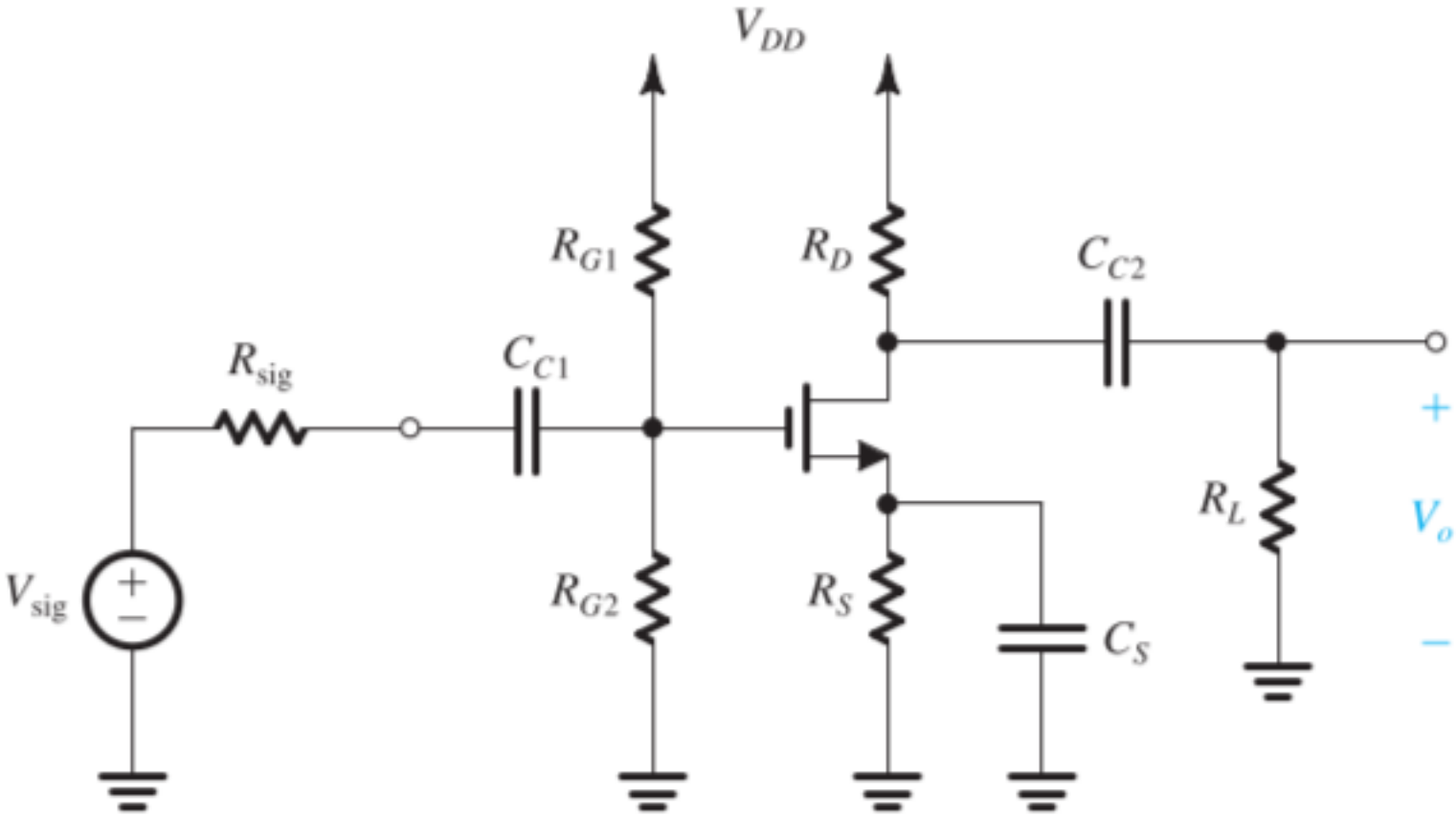
D 10.1 For the amplifier in Fig. 10.3(a), if $R_{G1} = 2\,\text{M}\Omega$, $R_{G2} = 1\,\text{M}\Omega$, and $R_{\text{sig}} = 200\,\text{k}\Omega$, find the value of the coupling capacitor C_{C1} (specified to one significant digit) that places the associated pole at 10 Hz or lower.



(a)

D 10.3 The amplifier in Fig. 10.3(a) is biased to operate at $g_m = 5\,\text{mA/V}$, and $R_S = 1.8\,\text{k}\Omega$. Find the value of C_S (specified to one significant digit) that places its associated pole at 100 Hz or lower. What are the actual frequencies of the pole and zero realized?

D 10.7 Figure P10.7 shows a current-biased CE amplifier operating at 100 μA from ±3-V power supplies. It employs $R_C = 20$ kΩ, $R_B = 200$ kΩ, and operates between a 20-kΩ source and a 10-kΩ load. The transistor $\beta = 100$. Select C_E first, for a minimum value specified to one significant digit and providing up to 80% of f_L where f_L is to be 100 Hz. Then choose C_{C1} and C_{C2}, each specified to one significant digit, and each contributing about 10% of f_L. What f_L results? What total capacitance is needed?

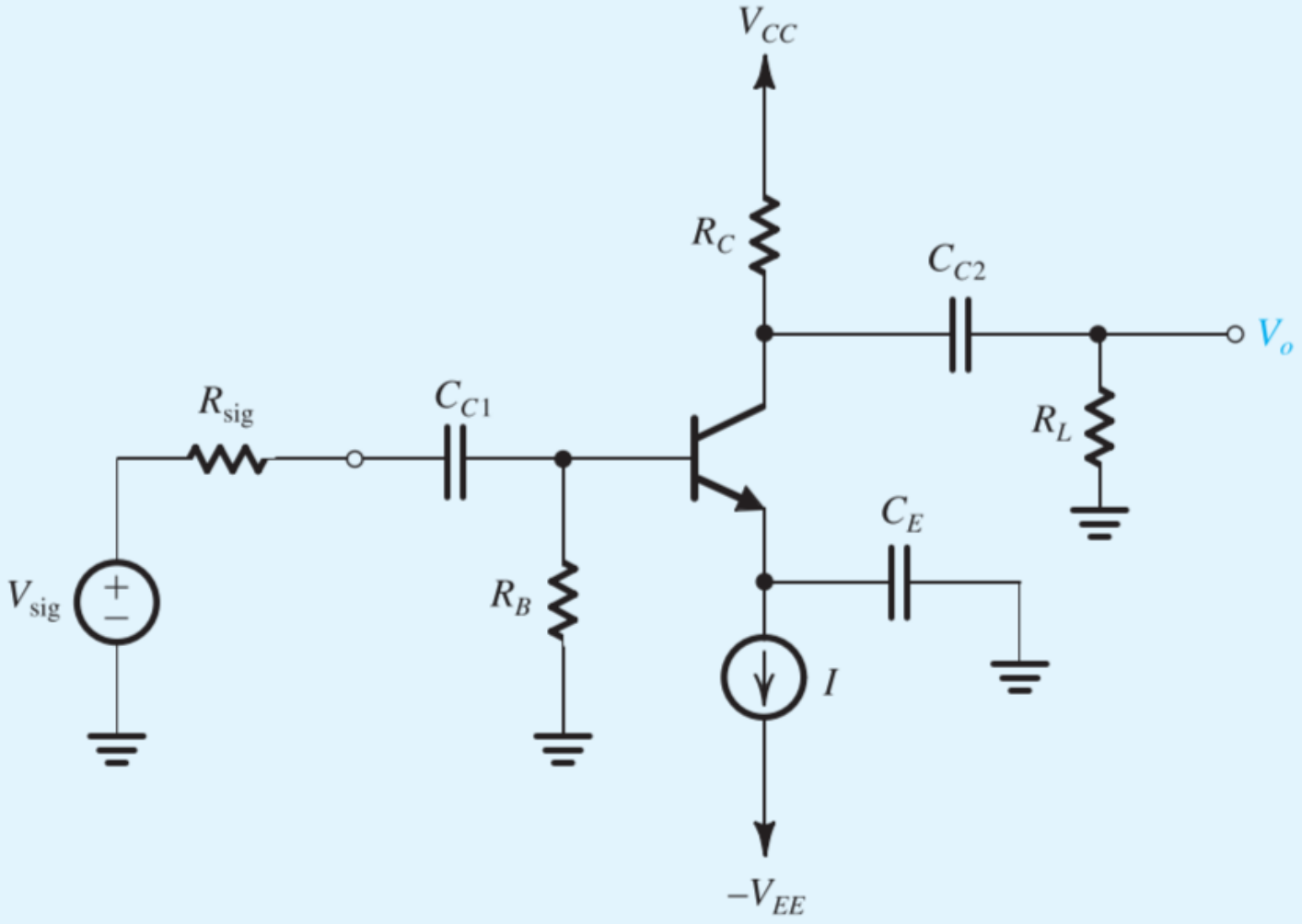


Figure P10.7

D *10.31 In a CS amplifier, such as that in Fig. 10.3(a), the resistance of the source $R_{sig} = 100\,\text{k}\Omega$, amplifier input resistance (which is due to the biasing network) $R_{in} = 100\,\text{k}\Omega$, $C_{gs} = 1\,\text{pF}$, $C_{gd} = 0.2\,\text{pF}$, $g_m = 3\,\text{mA/V}$, $r_o = 50\,\text{k}\Omega$, $R_D = 8\,\text{k}\Omega$, and $R_L = 10\,\text{k}\Omega$. Determine the expected 3-dB cutoff frequency f_H and the midband gain. In evaluating ways to double f_H, a designer considers the alternatives of changing either R_L or R_{in}. To raise f_H as described, what separate change in each would be required? What midband voltage gain results in each case?