Laboratory 4: Biasing of Bipolar Transistors

Preliminary Exercises

In lecture, we studied the relative properties of different biasing circuits. Of particular interest was the sensitivity of these various circuits to transistor parameters. To demonstrate these properties, we will design three biasing circuits using typical transistor parameters of β=100 and V_{BE}=0.7V, then see how changes in β (to 50 and 300) effect their performance.

1. Design and Compare Three Bias Circuits

Design the following bias circuits using transistor parameters of β=100 and V_{BE}=0.7V for npn transistors and V_{EB}=0.7V for pnp transistors. For all circuits, I_C and V_{CE} must meet the specified values within a tolerance of ±5%. For each circuit design, calculate I_C and V_{CE} from your chosen resistors and confirm that I_C and V_{CE} are within ±5% of the specifications. You should use only standard resistor values in your design, and each resistive element in the circuit should use only a single physical resistor (no series or parallel combinations). Standard resistor values have the following mantissas: 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, and 8.2.

(a) For the circuit in Fig. PL4.1(a), select the resistor values that establish an operating point of I_C=5mA and V_{CE}=6V.

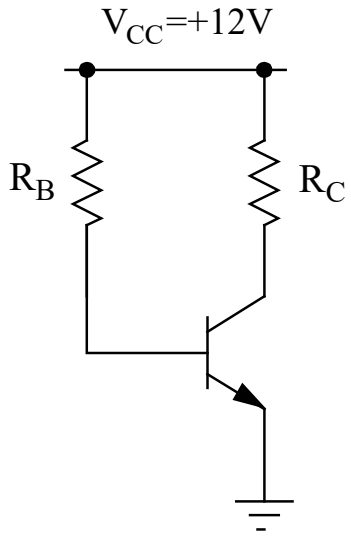


Figure PL4.1(a): Circuit 1

(b) For the circuit in Fig. PL4.1(b), select resistor values that establish an operating point of V_{CE}=5.5V and I_C=5mA. V_E should be around 2.3V.

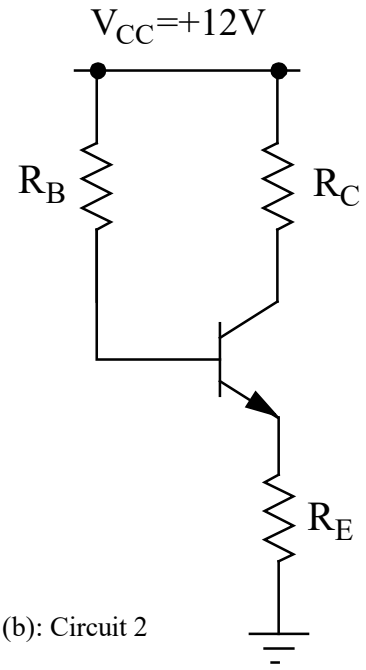


Figure PL4.1(b): Circuit 2

(c) Modify the circuit in part (b) as shown in Fig. PL4.1(c). This circuit should have the same operating point (V_{CE} and I_C). You should draw around 2.5 mA in the voltage divider formed by R_1 and R_2.

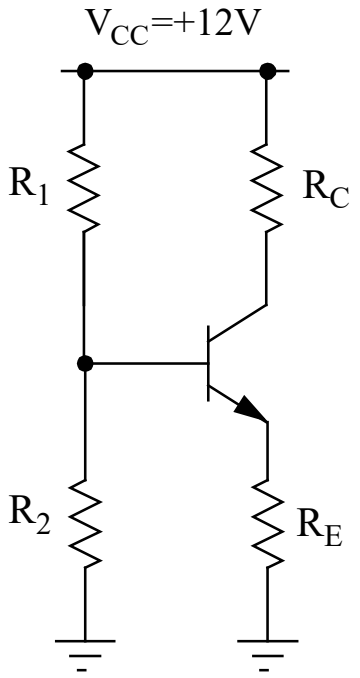


Figure PL4.1(c): Circuit 3

(d) Assume that we would like to bias pnp transistors to the same operating point as in the three circuits above. What simple circuit change (common to all three circuits) would be required?

2. Analysis of the Bias Circuits

(a) For each of the above circuits, compute the expected V_{CE} and I_C for β=50, 100, and 300. Use these computations to fill in the tables on the *Results Sheet for Preliminary Exercises*. You can assume that V_{BE}=0.7V for npn transistors and V_{EB}=0.7V for pnp transistors. If $V_{CE} \leq V_{CE}(\text{sat}) \approx 0.2\text{V}$, also enter "saturated".

(b) Based on the above analysis, rank the circuits you designed in terms of sensitivity to β. The specifications are I_C and V_{CE}.

(c) Briefly explain why each circuit performed as it did in terms of β sensitivity.

Laboratory 4: Biasing of Bipolar Transistors

Results Sheet for Preliminary Exercises

NAME: _____ **LAB SECTION:** _____

1. Design of Three Biasing Circuits

(a) R_B = _____, R_C = _____

(b) R_B = _____, R_C = _____ , R_E = _____

(c) R_1 = _____, R_2 = _____

R_C = _____, R_E = _____

(d) What circuit modification would be required? Justify.

2. Analysis of the Bias Circuits

Values of I_C (npn/pnp)

CIRCUIT	β=50		β=100		β=300	
	npn	pnp	npn	pnp	npn	pnp
1						
2						
3						

Values of V_{CE} (npn/pnp)

CIRCUIT	β=50		β=100		β=300	
	npn	pnp	npn	pnp	npn	pnp
1						
2						
3						

(b) Rank the circuit "Least Sensitive" to "Most Sensitive"

Least _____

_____

Most _____

(c) Justify.

Laboratory 4: Biasing of Bipolar Transistors

Laboratory Exercises

INTRODUCTION

Objectives

In this lab, we will design and build three different bias circuits for BJT's (Bipolar Junction Transistors). In our terminology, $\beta=\beta_{dc}$.

Summary of Procedures

(i) Design bias circuits around transistors with typical properties of $\beta=100$ and $V_{BE}=0.7V$ (for npn) or $V_{EB}=0.7V$ (for pnp).

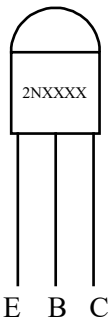
(ii) Build each circuit using a 2N3904, 2N2222, and a 2N3906.

(iii) Measure the operating point of each circuit and take data sufficient to estimate β and V_{BE}.

(iv) Use the HP 4155A/B/C to get β and β_{ac} near the bias point for each transistor used in "Circuit 3".

Materials Required

- HP 4155A/B/C (or HP 4145B) Semiconductor Parameter Analyzer



Transistor Pinout

- Proto-board
- Power Supplies
- DMM
- Assorted Resistors
- 2N2222 Transistor
- 2N3904 Transistor
- 2N3906 Transistor

PROCEDURE

Construct each of the circuits designed in the Preliminary Section using a 2N3904, 2N2222, and a 2N3906.

(a) For each circuit, evaluate the operating point (V_{CE} and I_C), being sure to use measured resistor values as needed. Record these values in the tables in the Results Sheet.

(b) Also take data sufficient to estimate the β of your 2N2222, 2N3904, and 2N3906. You only need to make measurements in one of the three circuits. Do not use a current meter unless you measure its internal resistance.

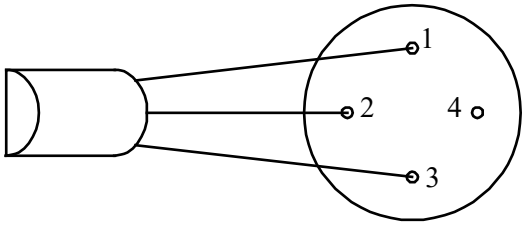
(c) Using the HP 4155A/B/C (see the procedure below), measure β and β_{ac} for your 2N2222, 2N3904, and 2N3906 **at the operating point for each transistor in Circuit 3, as measured in part (a).**

HP 4155A/B/C Instructions for Measurement of Bipolar Junction Transistor Characteristics

You will use the HP 4155A/B/C Semiconductor Parameter Analyzer to measure transistor characteristics (in this case, the common emitter current gains β and β_{ac}). Remember that you must obtain β and β_{ac} at the operating point (I_C and V_{CE}) corresponding to your results in Circuit 3.

The following procedure will make the necessary measurement and provide the required data plot. The HP 4155B has two types of keys: "hard" keys, which are dedicated buttons on the front panel, and a column of "soft" keys, just to the right of the screen. In the procedure below, a KEY is a hard key, and a KEY is a soft key. Note that you may have to use the EXTN (extension) soft key, which pages from one soft key menu to the next, to find some of the indicated soft key entries.

I. Connect your transistor to the test fixture as shown below (same for all three transistors):



1: Emitter: SMU3/VSU1 (CONST)

2: Base: SMU2 (VAR2)

3: Collector: SMU1 (VAR1)

II. For the npn transistors (2N3904 and 2N2222):

(1) CHAN to navigate to the "CHANNEL DEFINITION" screen. Name the channels according to the pins above. Be sure to set V_C to VAR1 (in voltage mode) and I_B to VAR2 (in current mode), which will allow you to sweep V_{CE} while stepping I_B. The datasheets for these transistors can be found on the course website.

(2) [MEAS] to get to the "SWEEP SETUP" screen. Set the sweep parameters so that V_{CE} is swept from 0V to 10V (in steps of at most 100mV) and I_B is swept from 0 to 100μA in 10μA steps. Be sure to ground V_E and set the compliances (both voltages and currents) to reasonable values given your expected bias voltages and currents.

(3) [DISPLAY] to get to the "DISPLAY SETUP" screen. Here you should setup the axes to plot I_C vs. V_{CE} while stepping I_B.

(4) [GRAPH/LIST] to get the "GRAPHICS PLOT" window.

(5) [SINGLE] to perform the measurement.

(6) [SCALING], [AUTOSCALING] if necessary to view the whole plot.

(7) [MARKER/ CURSOR], [MARKER OFF] to turn marker on (the soft key should now read [MARKER ON]); move it to the V_{CE} you measured for circuit 3 in part (a) with the knob.

(8) [MARKER SKIP] to move from curve to curve (different I_B's) in the characteristic until you find the I_C value closest to the *measured* I_C for circuit 3 in part (a). β is then I_C/I_B.

(9) If the closest value of I_C is *not* within ±0.5mA of your *measured* I_C, you must adjust the input values of I_B to come closer. You will do this by adjusting the starting value of I_B (originally set at 10μA), which will have the effect of shifting the measured characteristic up or down on the plot (depending on whether you increase or decrease, respectively, the starting value of I_B). You should change the starting value to be somewhere in the range of 5μA < I_B < 15 μA. You can come very close to the best correct value by estimating $\boldsymbol{\beta = \frac{I_C}{I_B}}$ at the value of I_C that came closest to your measured I_C.

(10) To measure β_{ac} you can use the combination of the marker and a cursor to find two different data points. Move the marker (the circle) to be at the data point corresponding to I_{B1}, I_{C1}, and V_{CE} (where V_{CE} should correspond to that obtained for the same transistor in circuit 3). Move the cursor (the cross) to be at the second data point corresponding to I_{B2}, I_{C2} (within $\pm 0.5\text{mA}$ of the I_C measured in circuit 3), and the same V_{CE}. Then

$$\beta = \frac{I_{C2}}{I_{B2}}; \beta_{ac} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}}$$

III. For the 2N3906, you should follow the same general procedure, adjusting your channel and variable assignments based on your knowledge of pnp transistors.

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Results Sheet for Laboratory Exercises

NAME: _____ **LAB SECTION:** _____

(a)

Values of V_{CE}

CIRCUIT	2N3906	2N3904	2N2222
1			
2			
3			

Values of I_C

CIRCUIT	2N3906	2N3904	2N2222
1			
2			
3			

(b) Values of β from circuit:

2N222 _____ , 2N3904_____, 2N3906_____

Which circuit did you choose to make your estimation? Why?

(c) Values of β/β_{ac} from HP 4155B (attach 3 annotated HP 4155B plots)

2N222 _____/_____, 2N3904 _____/_____, 2N3906 _____/_____

Briefly outline your measurements. (How were I_C, V_{CE}, and β measured and how was the HP 4155B used?)

Comment on the relative properties of each of the circuits used in this design. (Explain sensitivity to β for each circuit.)