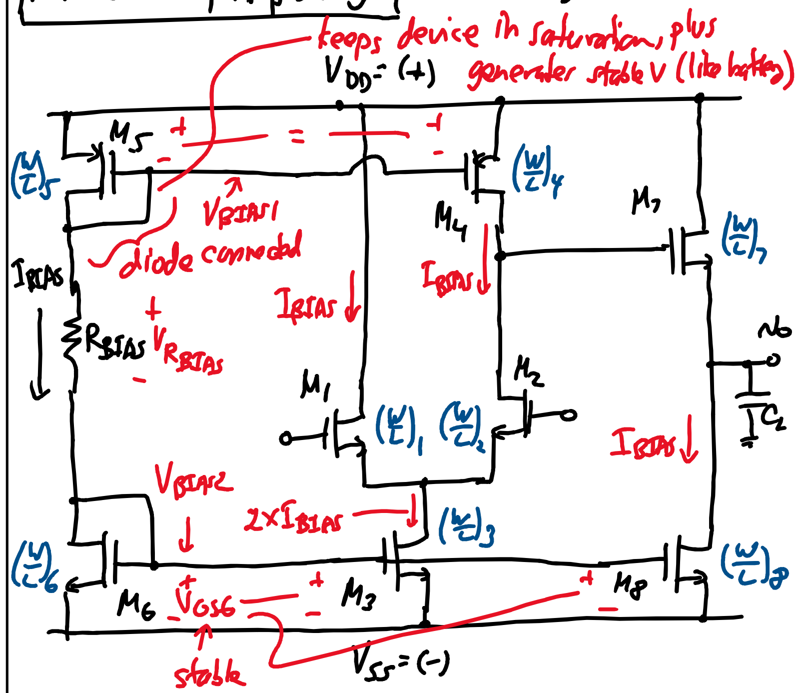
Lecture 36: Digital Circuits

- Announcements:
- HW#11 is online and due Tuesday, Dec. 10 (more than two weeks from now)
- Lab 6 online and due 5 p.m., Friday, Dec. 13
- ------------------------------------
- Lecture Topics:
  - Finish MOS Op Amp Analysis
  - Review of Digital Electronics
  - Definitions
  - MOS Inverter w/ Resistive Load
- ------------------------------------
- Last Time:
- Analyzing a simple CMOS op amp
- Now, finish this, then move on to digital circuits ...

An Actual Op Amp Design (in CMOS)



Biasing:

$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$ → to eliminate V_{OS}

$\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_5$ → for $I_{D4} = I_{D5} = I_{BIAS}$

$\left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_6$ → for $I_{D8} = I_{D6} = I_{BIAS}$

$\left(\frac{W}{L}\right)_3 = 2\times\left(\frac{W}{L}\right)_6$ → for $I_{D3} = 2I_{D6} = 2I_{BIAS}$

To Specify I_{BIAS} → specify R_{BIAS}:

$$R_{BIAS} = \frac{V_{R_{BIAS}}}{I_{BIAS}} = \frac{V_{DD} - |V_{GS5}| - V_{GS6} - V_{SS}}{I_{BIAS}}$$

$$I_{DS} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_5 (|V_{GS5}| - |V_{tp}|)^2$$

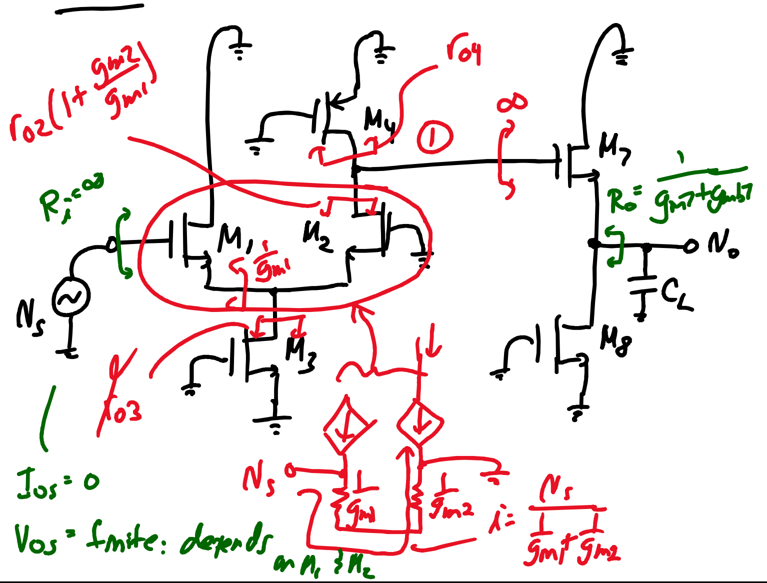
↳ $$|V_{GS5}| = |V_{tp}| + \sqrt{\frac{2 I_{BIAS}}{\mu_p C_{ox}(W/L)_5}}$$

Similarly: $$V_{GS6} = V_{tn} + \sqrt{\frac{2 I_{BIAS}}{\mu_n C_{ox}(W/L)_6}}$$

↳ Pick an I_{BIAS} → Get the needed R_{BIAS}

Gain ⇒ focus on the signal path only!

S.S. Ckt:



$$\frac{v_o}{v_s} = \frac{v_①}{v_s}\cdot\frac{v_o}{v_①}$$

$$\frac{v_①}{v_s} = G_{m\,diff} R_① = \frac{1}{\frac{1}{g_{m1}}+\frac{1}{g_{m2}}}\left[r_{o4} \,||\, r_{o2}\left(1+\frac{g_{m1}}{g_{m2}}\right)\right]$$

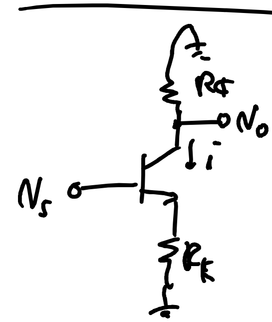
($\frac{1}{\frac{1}{g_{m1}}+\frac{1}{g_{m2}}} = G_{m\,diff}$; $\left(1+\frac{g_{m1}}{g_{m2}}\right) = 2$)

$$= \frac{1}{2} g_{m1}(r_{o4} \,||\, 2r_{o2})$$

$$\frac{v_o}{v_①} = \frac{g_{m7}}{g_{m7}+g_{mb7}} \simeq 1$$

$$\therefore \frac{v_o}{v_s} = +\frac{1}{2} g_{m1}(r_{o4} \,||\, 2r_{o2})$$

This is A_v = the op amp midband gain.

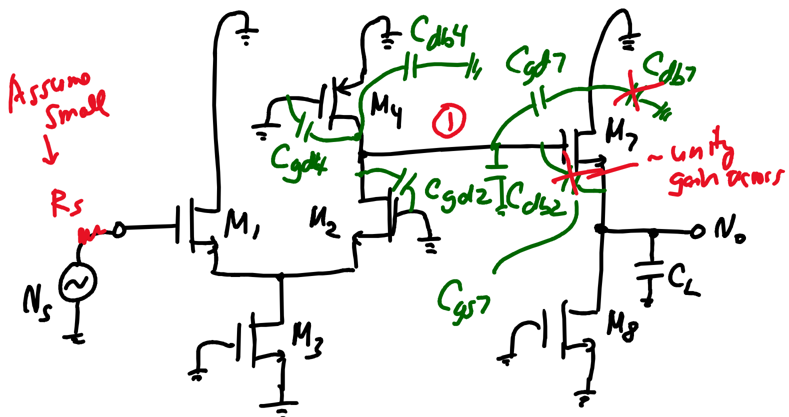


$$\frac{v_o}{v_s} = -G_m R_C$$

$$G_m = \frac{i}{v_s} = \frac{g_m}{1+g_m R_E}$$

High Freq. Cut-off ⇒ focus on the highest impedance node → node ①

H.F.S.S. Ckt:

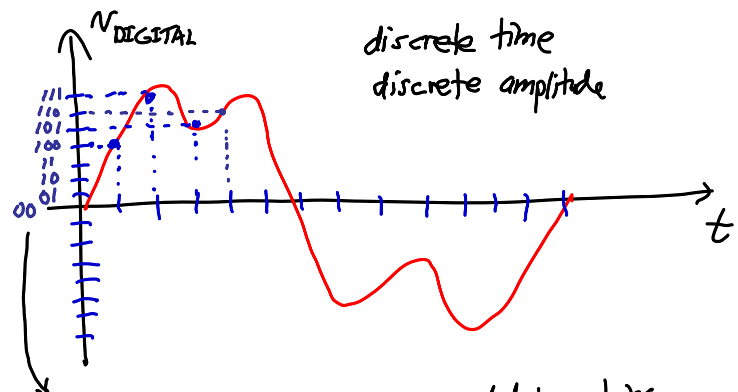


$$\omega_H = \frac{1}{(r_{o4} \| (2r_{o2}))\{C_{gd2} + C_{gd4} + C_{db4} + C_{db2} + C_{gd7}\}}$$

(this dominates the first pole)

⇒ Continue in EE140 . . .

- So far, our focus has been on analog amplifiers that process analog signals
- Earlier in the class, however, we looked at different signal types: analog, sampled-data, and digital
- Digital Signal:

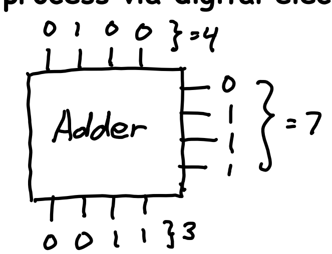


These values can now be encoded in a binary representation and processed via digital electronics

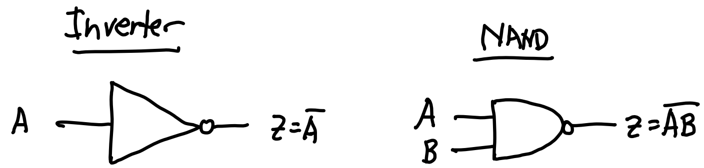
⇒ Problem: Lose information through quantization

$$\text{Lost Info} \propto \frac{1}{\#\text{ of levels}}$$

- With enough levels, we can reduce quantization error to unnoticeable levels
- The process via digital electronics, e.g., adder



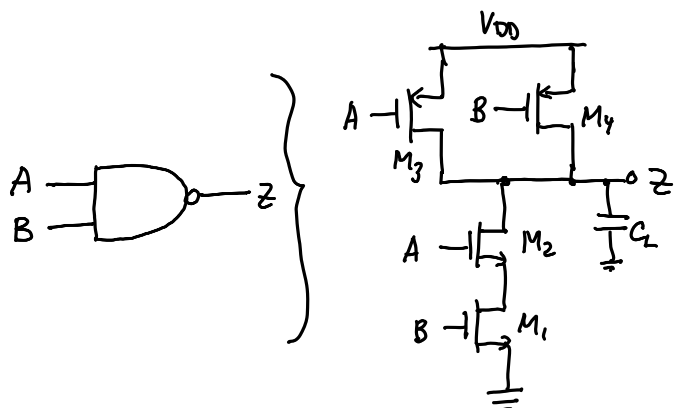
- This class won't cover the design of this adder
- For now, suffice it to say that one way to design the adder is to put together a circuit of gates: inverters, NAND gates, NOR gates, etc.



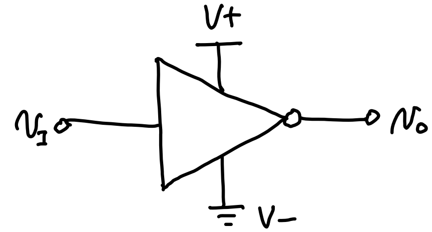
A	$Z=\bar{A}$
0	1
1	0

A	B	$Z=\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

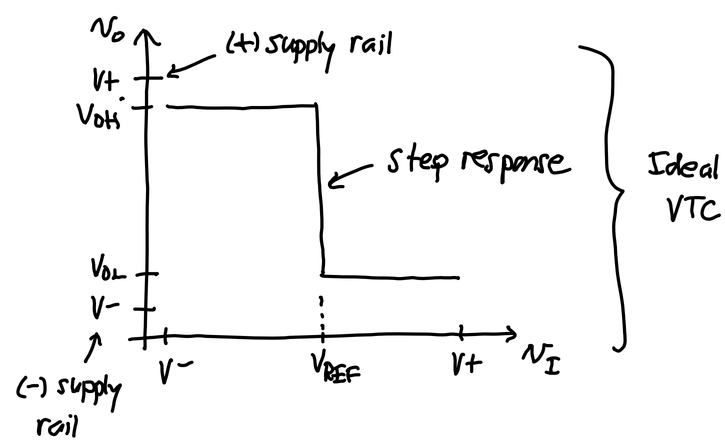
- Here, 0 → low voltage, 1 → high voltage
- If you have a NAND gate, you can make any digital function, including the adder above
- The NAND gate is a digital circuit that uses 4 transistors

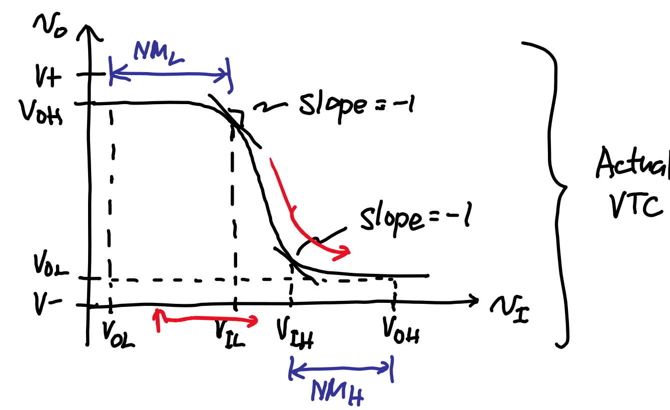


- The key to understanding this circuit starts with understanding a simpler circuit: the inverter



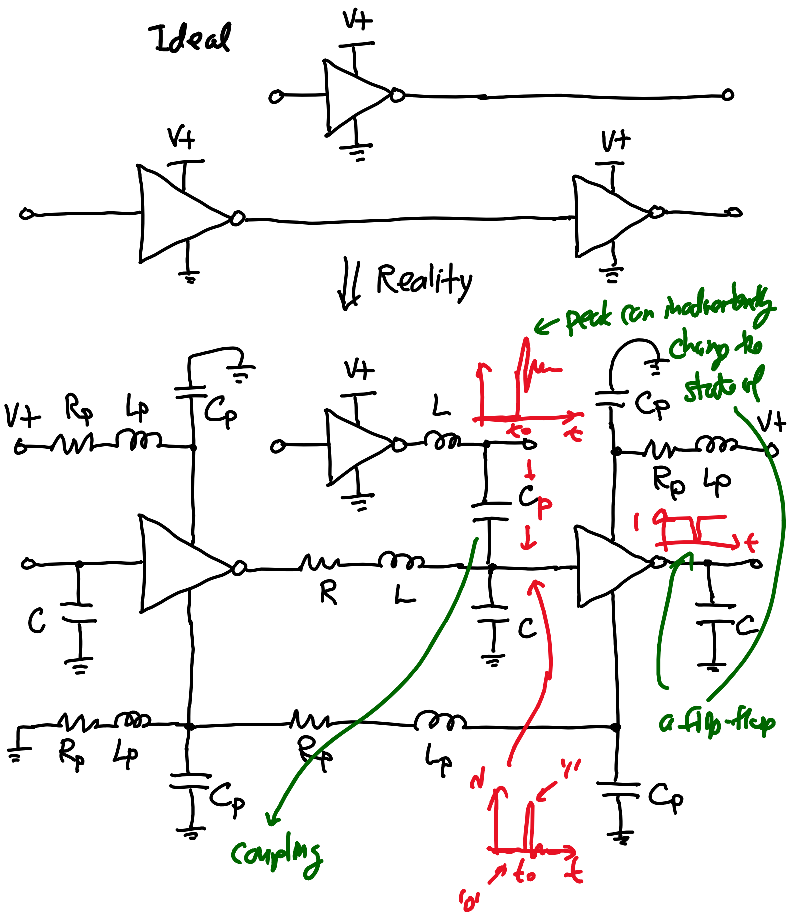
Voltage Transfer Characteristic (VTC)



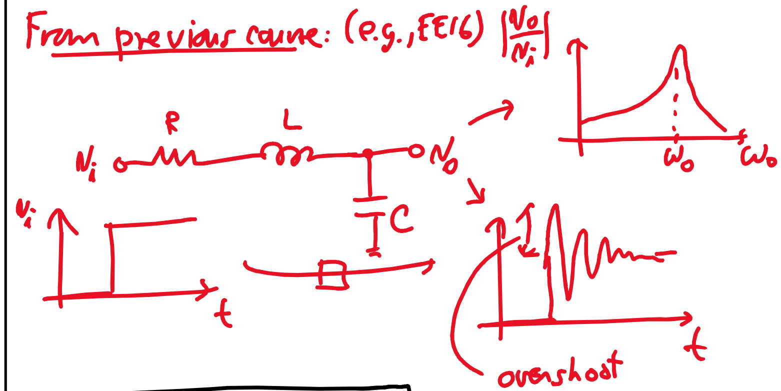


- V_{OL} = output low voltage (0)
- V_{OH} = output high voltage (1)
- V_{IL} = max. input voltage recognized as input low
- V_{IH} = min. input voltage recognized as input high
- $NM_L = V_{IL} - V_{OL}$ = noise margin low
- $NM_H = V_{OH} - V_{IH}$ = noise margin high

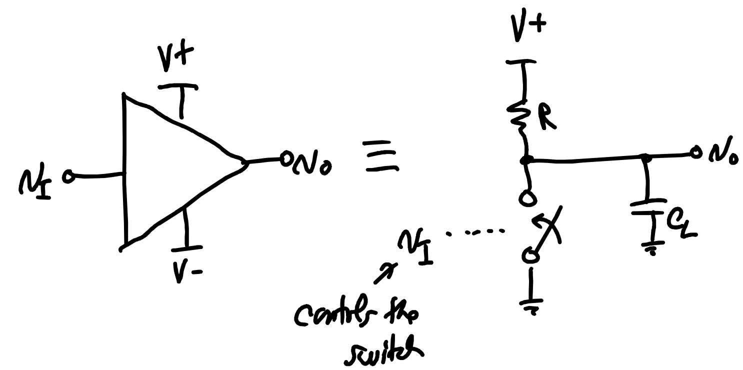
Why noise margins?



From previous course: (e.g., EE16)



Resistively-Loaded Inverter



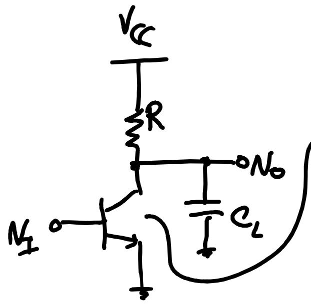
Cases:

① switch open: C_L charges to V+

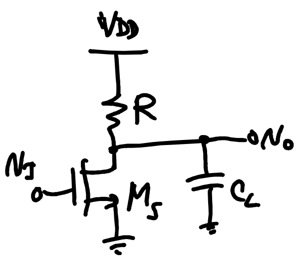
② switch closed: C_L discharges to ground

Transistor Inverter w/ Resistive Load

⇒ use Xristor as a switching device → allowing it to handle large signals



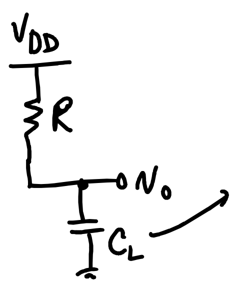
bipolar Xristor (first inverters used bipolar technology)
But… not as good as MOS for digital ckts.
↳ reasons: cost & power consumption



Find V_{OH} & V_{OL}.
(for this resistively-loaded MOS Inverter)

V_{OH}: $v_I \le V_{IL}$ → say $v_{IL} = 0V$

⇒ M_S off

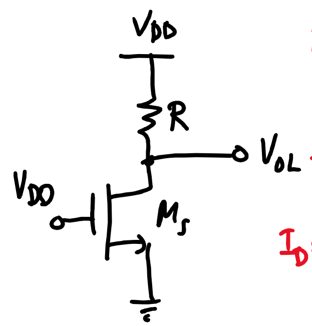


C_L charges to $v_O = V_{DD} = V_{OH}$

V_{OL}: $v_I = V_{IH}$ → say $v_I = V_{DD}$

⇒ M_S on

⇒ in steady-state:



For M_S: $V_{GSS} - V_{TNS} = V_{DD} - V_{TNS} > V_{OL}$

∴ M_S is linear

→ $V_{OL} = V_{DD} - I_D R$

$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)_S \left(V_{DD} - V_{TNS} - \frac{V_{OL}}{2}\right) V_{OL}$

$$V_{OL} = V_{DD} - \mu_n C_{ox}\left(\frac{W}{L}\right)_S (V_{DD} - V_{TNS}) V_{OL} + \frac{\mu_n C_{ox}\left(\frac{W}{L}\right)_S}{2} V_{OL}^2$$

⇒ solve quadratic for V_{OL}