Lecture 38: CMOS Noise Margins

- Announcements:
- HW#11 is online and due Tuesday, Dec. 10
- Lab 6 online and due 5 p.m., Friday, Dec. 13
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- Lecture Topics: (over the next few days)
  - MOS Inverter w/ Resistive Load
  - Static CMOS Inverter Behavior
    - V_{OL} and V_{OH}
    - V_{IL} and V_{IH}
  - Dynamic CMOS Inverter Behavior
    - Propagation Delay
    - Capacitance
  - Astable Ring Oscillator
  - CMOS Inverter Propagation Delay
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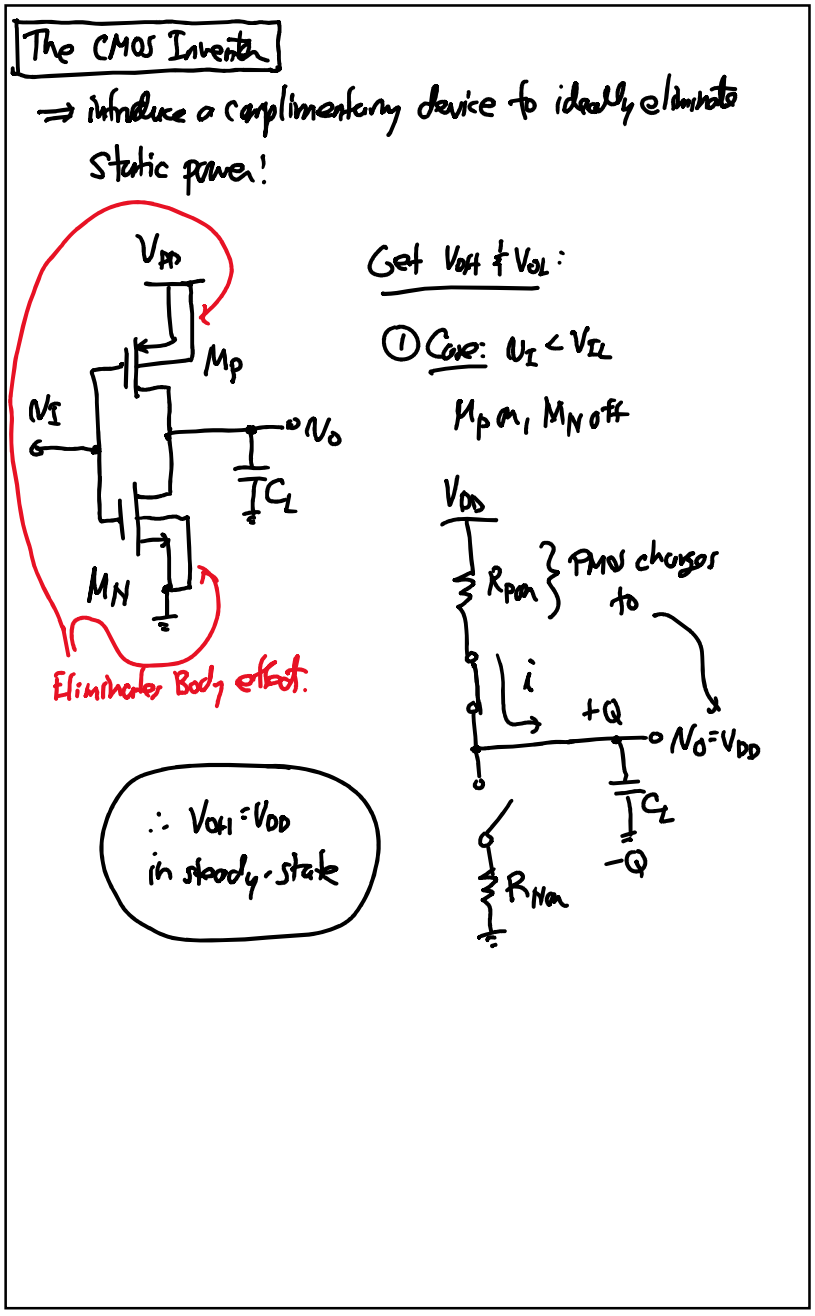
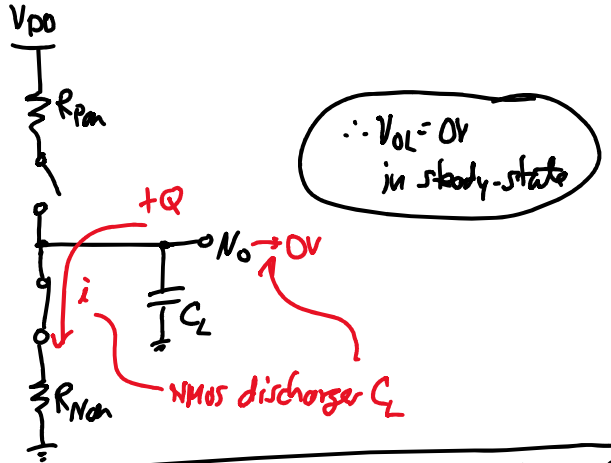
- Last Time:
- Covered CMOS inverter outputs (V_{OL} and V_{OH})
- Now, get input ranges (that then determine noise margins)...



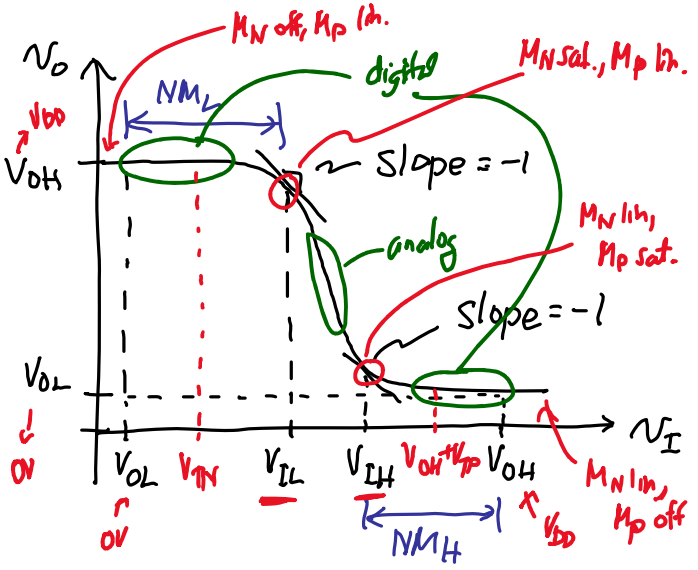
② Case: $V_I > V_{IH}$

M_P off, M_N on



∴ $V_{OL} = 0V$ in steady-state

Determination of the Voltage Transfer Characteristic (VTC)

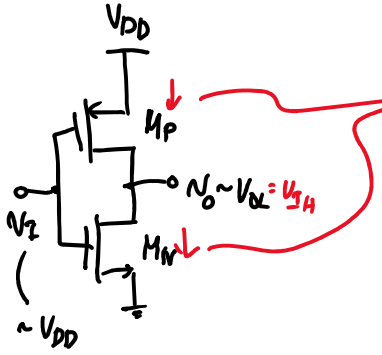


Already know $V_{OL} = 0V$, $V_{OH} = V_{DD}$. Now, find $V_{IL}, V_{IH}, NM_L, NM_H$. } for the CMOS inverter

V_{IH}:

M_N linear w/ $V_{GS} = V_I, V_{DS} = V_O$

M_P saturated w/ $V_{SG} = V_{DD} - V_I$, $V_{SD} = V_{DD} - V_O$



Thus: (equating drain currents)

$$i_{DSN}(\text{lin}) = i_{SDP}(\text{sat.})$$

$$\underbrace{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}_{k_n}\left(V_I - V_{TN} - \frac{V_O}{2}\right)V_O = \underbrace{\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_p}_{k_p}\left(V_{DD} - V_I + V_{TP}\right)^2$$

$$\left[K_R = k_n/k_p\right] \Rightarrow K_R\left(2V_I - 2V_{TN} - V_O\right)V_O = \left(V_{DD} - V_I + V_{TP}\right)^2$$

Solve for V_O: ... algebra ...

$$v_O = v_I - V_{TN} \mp \sqrt{(v_I - V_{TN})^2 - \frac{(V_{DD} - v_I + V_{TP})^2}{K_R}}$$

$\left[\frac{dv_O}{dv_I} = -1,\ v_I = V_{IH}\right] \Rightarrow$ Lots of math ... using Mathematica ...

$$V_{IH} = \frac{2K_R(V_{DD} - V_{TN} + V_{TP})}{(K_R - 1)\sqrt{1 + 3K_R}} - \frac{(V_{DD} - K_R V_{TN} + V_{TP})}{K_R - 1}$$

$$= \frac{2K_R(V_{DD} - V_{TN} - |V_{TP}|)}{(K_R - 1)\sqrt{1 + 3K_R}} - \frac{(V_{DD} - K_R V_{TN} - |V_{TP}|)}{K_R - 1}$$

one condensed form seen in literature

Problem: Not useful for the popular case when $K_R = 1$, i.e., $K_N = K_P$

For $K_R = 1$, better to go back to the original constraining equations:

For $K_R = 1$:

$$(2v_I - 2V_{TN} - v_O)v_O = (V_{DD} - v_I + V_{TP})^2$$

$$(2v_I - 2V_{TN} - v_O)\frac{dv_O}{dv_I} + \left(2 - \frac{dv_O}{dv_I}\right)v_O = 2(V_{DD} - v_I + V_{TP})(-1)$$

$\left[\frac{dv_O}{dv_I} = -1,\ v_I = V_{IH}\right] \Rightarrow$

*

$$(2v_I - 2V_{TN} - v_O)(-1) + 3v_O = -2V_{DD} + 2v_I - 2V_{TP}$$

↓ math

$$2v_O + V_{TN} + V_{TP} + V_{DD} = 2V_{IH}$$

$$V_{IH} = \frac{2v_O + V_{TN} + V_{TP} + V_{DD}}{2} \rightarrow v_O = \frac{1}{2}(2V_{IH} - V_{TN} - V_{TP} - V_{DD})$$

$[v_I = V_{IH}] \rightarrow$ Lots of math ...

$$V_{IH} = \frac{5V_{DD} + 3V_{TN} + 5V_{TP}}{8}$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH}$$

$$\therefore NM_H = \frac{3V_{DD} - 3V_{TN} - 5V_{TP}}{8}$$

Important Case:

⇒ NMOS & PMOS have identical strength

⇒ $V_{TN} = V_t$, $V_{TP} = -V_t$ (symmetrical V_t magnitudes)

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t),\quad NM_H = \frac{1}{8}(3V_{DD} + 2V_t)$$

- Remarks:
- K_R=1 can can be an important case when one wants the switching point to be at $V_{DD}/2$
- To get this case, one must size the PMOS bigger than the NMOS to give the former equal strength
- But if area is important (for cost reasons), then a designer will choose to use minimum-size devices, in which case the PMOS will not be as strong as the NMOS
  - The switch point will shift a bit from the midpoint of the supply
  - K_R not equal to 1

V_{IL}:

M_N saturated w/ $V_{GS}=V_I$, $V_{DS}=V_O$

M_P linear w/ $V_{SG}=V_{DD}-V_I$, $V_{SD}=V_{DD}-V_O$

[Again, equate to drain currents] ⇒

$$I_{SDP(lin.)} = I_{DSN(sat.)}$$

$$K_R\left(V_{DD}-V_I+V_{TP}-\frac{V_{DD}-V_O}{2}\right)(V_{DD}-V_O)=\frac{K_n}{2}(V_I-V_{TN})^2$$

$\left[\frac{dV_O}{dV_I}=-1,\ V_I=V_{IL}\right]$ ⇒ Again, lots of math ...

$$V_{IL}=\frac{2\sqrt{K_R}(V_{DD}-V_{TN}+|V_{TP}|)}{(K_R-1)\sqrt{K_R+3}}-\frac{(V_{DD}-K_R V_{TN}+|V_{TP}|)}{K_R-1}$$

$$=\frac{2\sqrt{K_R}(V_{DD}-V_{TN}-|V_{TP}|)}{(K_R-1)\sqrt{K_R+3}}-\frac{(V_{DD}-K_R V_{TN}-|V_{TP}|)}{K_R-1}$$

↳ Again, not useful for $K_R=1$

Using a similar procedure to V_{IH}, can get for $K_R=1$:

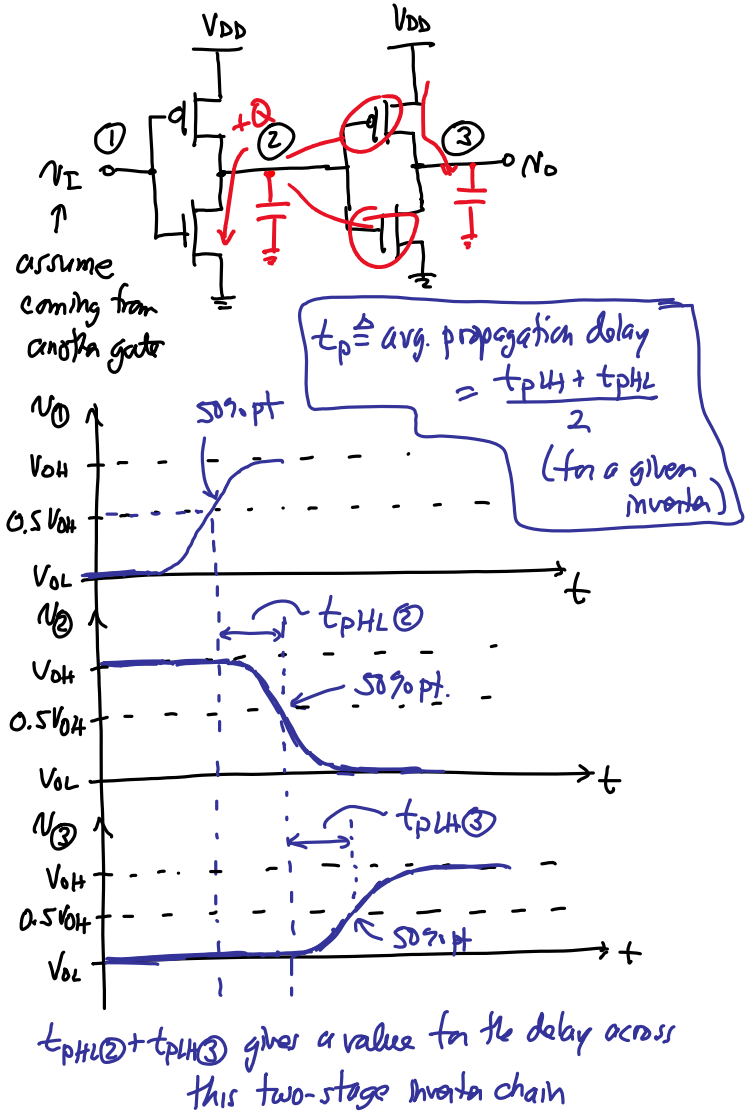
$$V_{IL}=\frac{3V_{DD}+5V_{TN}+3V_{TP}}{8},\quad NM_L=V_{IL}$$

... and for $K_R=1$, $V_{TN}=V_t$, $V_{TP}=-V_t$

$$V_{IL}=\frac{1}{8}(3V_{DD}+2V_t)=NM_L$$

Dynamic Behavior of the CMOS Inverter

Propagation Delay -

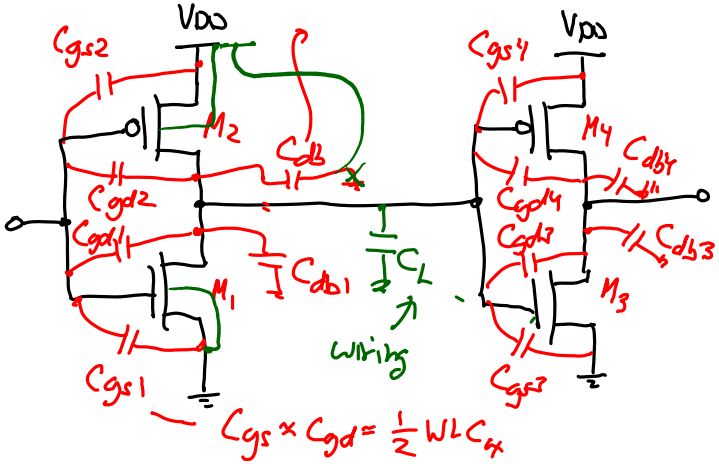


tpHL② + tpLH③ gives a value for the delay across this two-stage inverter chain

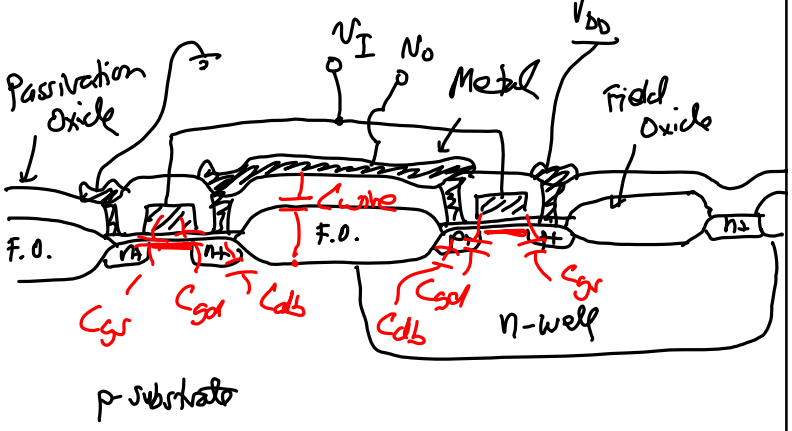
- **Remarks**
- Propagation delay is the delay experienced by a signal passing through a gate as measured between the 50% transition points between input and output waveforms
- In general, a gate displays different response times for rising and falling input waveforms
- Thus, define:
  - t_{pLH}: response time of a gate making a low→high output transition
  - t_{pHL}: response time of a gate making a high→low output transition
- Propogation delay then defined as the average of t_{pLH} and t_{pHL}
- What causes switching delay?
  - Finite current transistor current drive (i.e., finite on resistance R_{on}
  - Output node capacitance

Capacitance

$$C_{db} = \frac{C_{db0}}{\sqrt{f(V_{DB})}} \cdot \frac{C_{db0}}{\left(1 + \frac{V_{DB}}{\Phi_J}\right)^m}$$



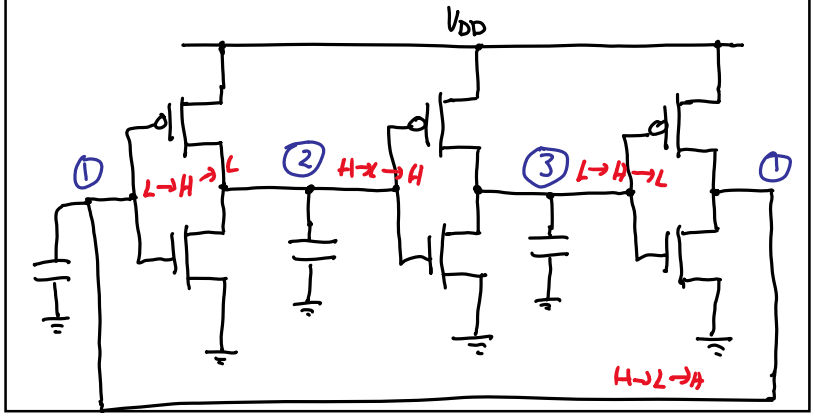
Actual CMOS (old) (an inverter)

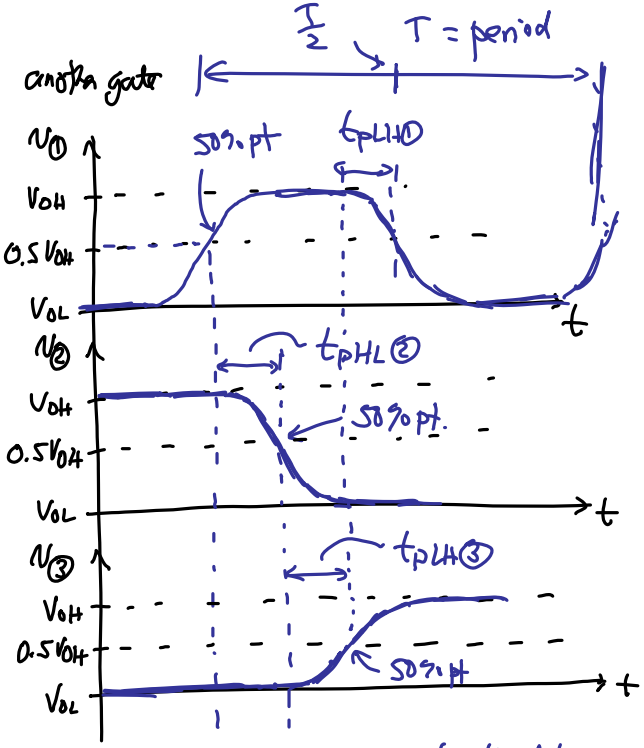


⇒ take EE143 to learn MORE!!!

Astable Ring Oscillator

⇒ what is an oscillator? → a device that puts out a stable frequency!





$t_{pHL②} + t_{pLH③}$ gives a value for the delay across this two-stage inverter chain

$\frac{1}{2}T = t_{p①} + t_{p②} + t_{p③}$

[Identical & symmetric inverters] ⇒

$t_p = t_{p①} = t_{p②} = t_{p③}$

$\Rightarrow \frac{1}{2}T = Nt_p \rightarrow T = 2Nt_p \Rightarrow f_o = \frac{1}{2Nt_p}$

oscillation freq.

N = no. of inverters