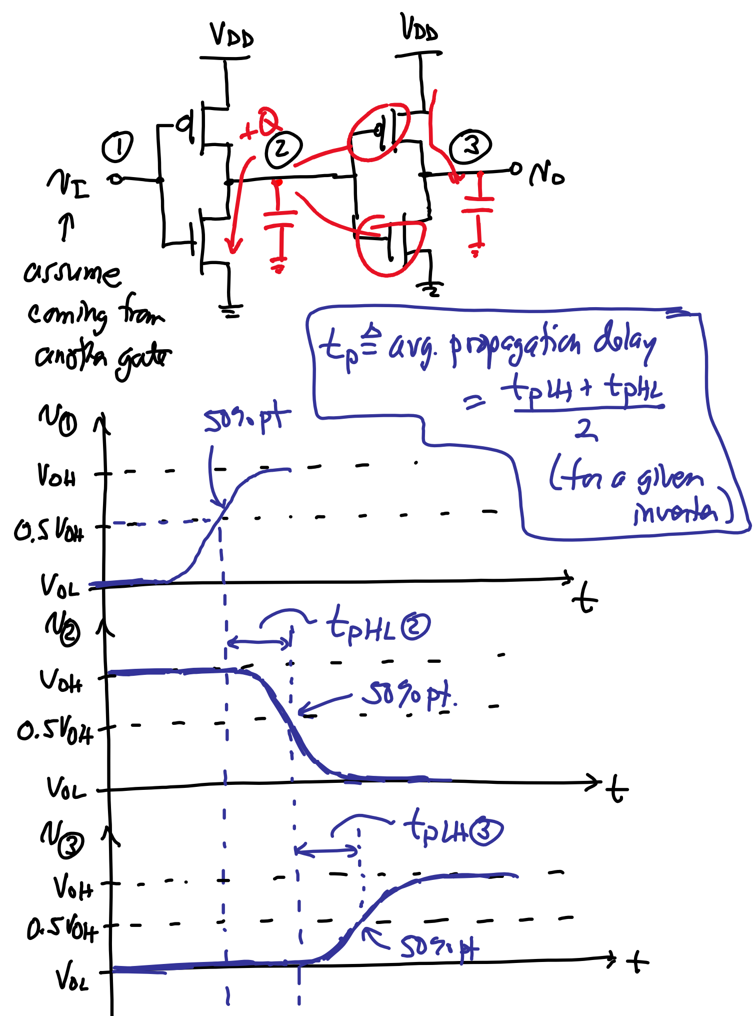
Lecture 39: Propagation Delay & Wrap Up

- **Announcements**:
- HW#11 is online and due Tuesday, Dec. 10
- Lab 6 online and due 5 p.m., Friday, Dec. 13
- Will go through Final Exam Information and pass out last year's final exam
- ------------------------------------
- Lecture Topics: (over the next few days)
  - MOS Inverter w/ Resistive Load
  - Static CMOS Inverter Behavior
    - V_{OL} and V_{OH}
    - V_{IL} and V_{IH}
  - Dynamic CMOS Inverter Behavior
    - Propagation Delay
    - Capacitance
  - Astable Ring Oscillator
  - CMOS Inverter Propagation Delay
- ------------------------------------
- **Last Time**:
- Started propagation delay
- Now, finish this and finish the course …

Dynamic Behavior of the CMOS Inverter

Propagation Delay –

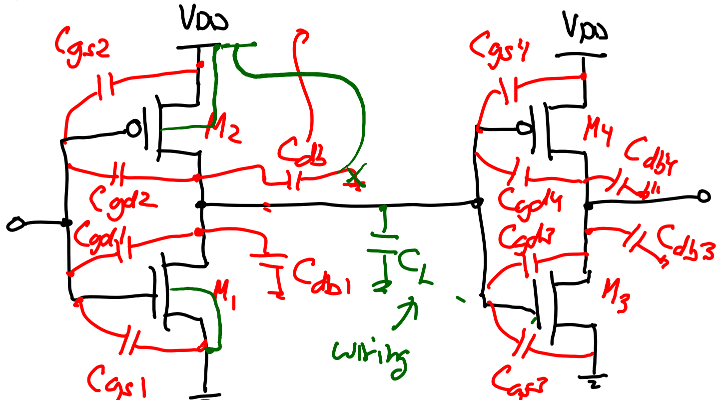


t_{pHL}② + t_{pLH}③ gives a value for the delay across this two-stage inverter chain

- Remarks
- Propagation delay is the delay experienced by a signal passing through a gate as measured between the 50% transition points between input and output waveforms
- In general, a gate displays different response times for rising and falling input waveforms
- Thus, define:
  - t_{pLH}: response time of a gate making a low→high output transition
  - t_{pHL}: response time of a gate making a high→low output transistion
- Propogation delay then defined as the average of t_{pLH} and t_{pHL}
- What causes switching delay?
  - Finite current transistor current drive (i.e., finite on resistance R_{on}
  - Output node capacitance

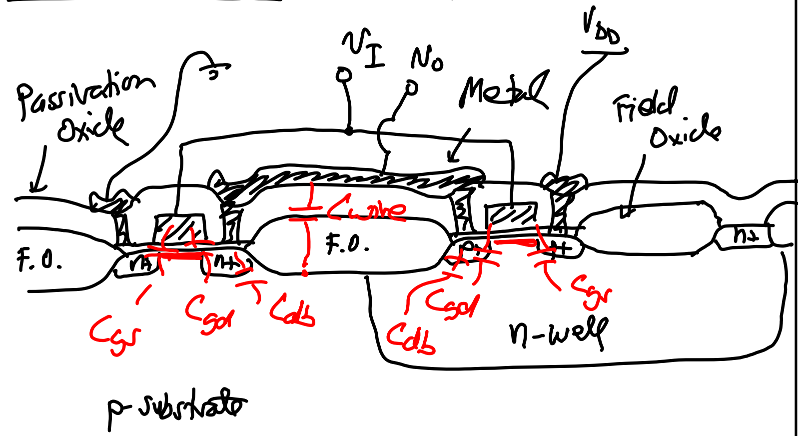
Capacitance

$$C_{db} = \frac{C_{db0}}{\sqrt{f(V_{DB})}} \cdot \frac{C_{db0}}{\left(1 + \frac{V_{DB}}{\phi_J}\right)^m}$$



$C_{gs} \approx C_{gd} = \frac{1}{2} W L C_{ox}$

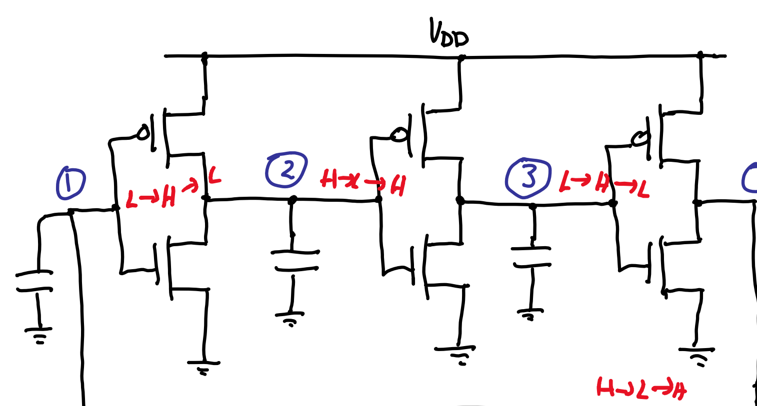
Actual CMOS (old) (an inverter)

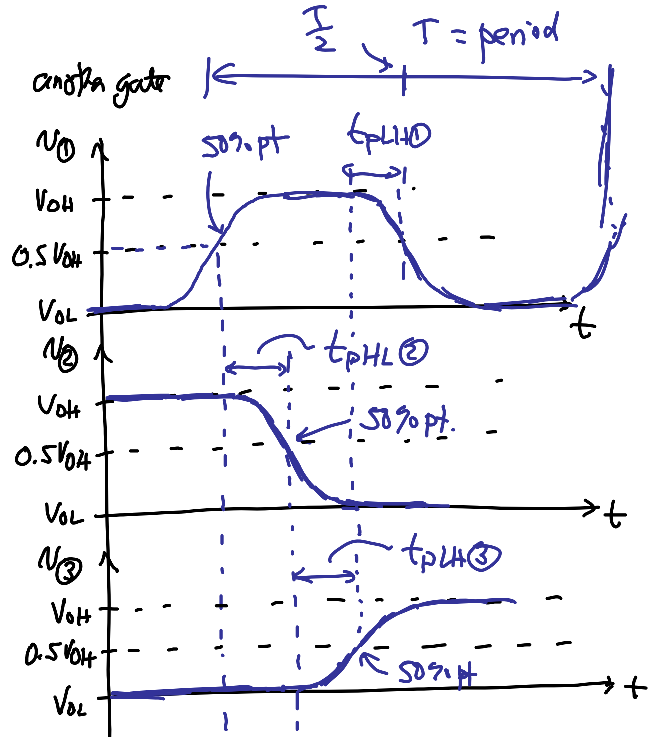


⇒ take EE143 to learn MORE!!!

Astable Ring Oscillator

⇒ what is an oscillator? → a device that puts out a stable frequency!





$t_{pHL②} + t_{pLH③}$ gives a value for the delay across this two-stage inverter chain

$\frac{1}{2}T = t_{p①} + t_{p②} + t_{p③}$

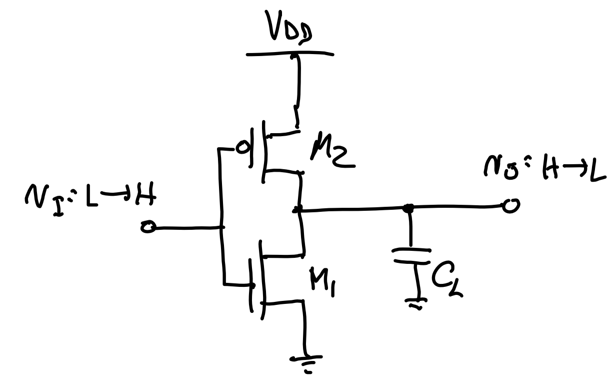
[identical & symmetric inverters] ⇒

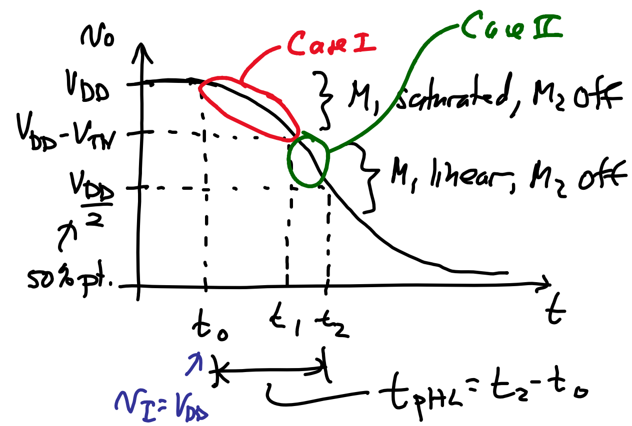
$t_p = t_{p①} = t_{p②} = t_{p③}$

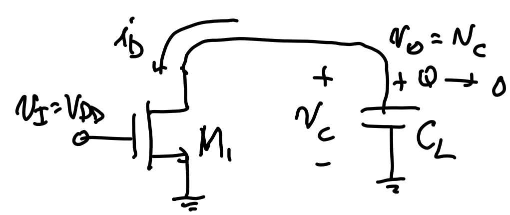
$\therefore \Rightarrow \frac{1}{2}T = N t_p \rightarrow T = 2N t_p \Rightarrow f_o = \frac{1}{2N t_p}$

(N = no. of inverters; f_o = oscillation freq.)

Propagation Delay in CMOS Inverters







Case: $v_O \ge V_{DD}-V_{TN}$ → M_1 saturated, M_2 off

Case I

$$i_{D(sat)} = \frac{k_n}{2}(V_{GS}-V_{TN})^2 = -C_L\frac{dv_C}{dt}$$

$$dt = \frac{-2C_L\,dv_C}{k_N(v_{GS}-V_{TN})^2} = \frac{-2C_L\,dv_C}{k_N(V_{DD}-V_{TN})^2}$$

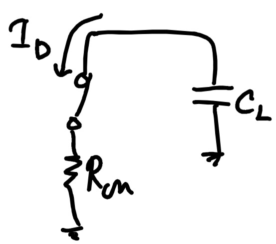
$$[v_{GS} = V_{OH} = V_{DD} = v_I]$$

$$\int_{t_0}^{t_1} dt = \int_{V_{DD}}^{V_{DD}-V_{TN}} -\frac{2C_L\,dv_C}{k_N(V_{DD}-V_{TN})^2}$$

$$(t_1-t_0) = -\frac{2C_L}{k_N(V_{DD}-V_{TN})^2}(V_{DD}-V_{TN}-V_{DD})$$

$$(t_1-t_0) = \frac{2C_L}{k_N(V_{DD}-V_{TN})}\frac{V_{TN}}{V_{DD}-V_{TN}} = 2C_L R_{on}\frac{V_{TN}}{V_{DD}-V_{TN}} = (t_1-t_0)$$

effective "on resistance" of the Xsistor → $R_{on} = \frac{1}{k_N(V_{DD}-V_{TN})}$



Case 2: $v_O < V_{DD}-V_{TN}$ → M_1 linear

$$i_D(lin) = -C_L\frac{dv_C}{dt}$$

$$k_N\left(v_{GS}-V_{TN}-\frac{v_{DS}}{2}\right)v_{DS} = -C_L\frac{dv_C}{dt}$$

$$[v_{DS}=v_C,\ v_{GS}=V_{DD}] \Rightarrow \left\{k_N\left(V_{DD}-V_{TN}-\frac{v_C}{2}\right)v_C = -C_L\frac{dv_C}{dt}\right\}\times 2$$

$$\int_{t_1}^{t_2}\frac{k_N}{2C_L}dt = -\int_{V_1}^{V_2}\frac{dv_C}{[2(V_{DD}-V_{TN})-v_C]v_C}$$

$$\left[\int\frac{dx}{(a-x)x} = \frac{1}{a}\ln\left(\frac{x}{a-x}\right)\right]$$

$$\left[V_2 = \frac{V_{DD}}{2},\ V_1 = V_{DD}-V_{TN}\right]$$

$$\frac{k_N}{2C_L}(t_2-t_1) = -\frac{1}{2(V_{DD}-V_{TN})}\ln\left[\frac{v_C}{2(V_{DD}-V_{TN})-v_C}\right]\Bigg|_{V_{DD}-V_{TN}}^{\frac{V_{DD}}{2}}$$

⋮ algebra

$$= -\frac{1}{2(V_{DD}-V_{TN})}\ln\left[\frac{V_{DD}}{4V_{DD}-4V_{TN}-V_{DD}}\right]$$

$$(t_2-t_1) = \frac{C_L}{k_N(V_{DD}-V_{TN})}\ln\left[\frac{4(V_{DD}-V_{TN})-V_{DD}}{V_{DD}}\right]$$

$$(t_2 - t_1) = \frac{C_L}{k_N(V_{DD} - V_{TN})} \ln\left[\frac{4(V_{DD} - V_{TN})}{V_{DD}} - 1\right]$$

$$(t_2 - t_1) = R_{on} C_L \ln\left[\frac{4(V_{DD} - V_{TN})}{V_{DD}} - 1\right]$$

$$t_{pHL} = (t_2 - t_1) + (t_1 - t_0) = (t_2 - t_0)$$

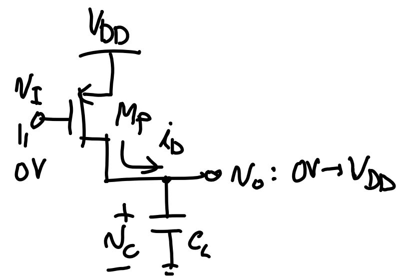
$$= R_{on} C_L \left\{ \ln\left(\frac{4(V_{DD} - V_{TN})}{V_{DD}} - 1\right) + \frac{2V_{TN}}{V_{DD} - V_{TN}} \right\} = t_{pHL}$$

where $R_{on} = \frac{1}{k_N(V_{DD} - V_{TN})}$

$\hookrightarrow t_{pHL} = R_{on} C_L \times f(V_{DD}, V_{TN})$

t_{pLH}: output: L→H

→ connect C_L to V_{DD} → PMOS on, NMOS off



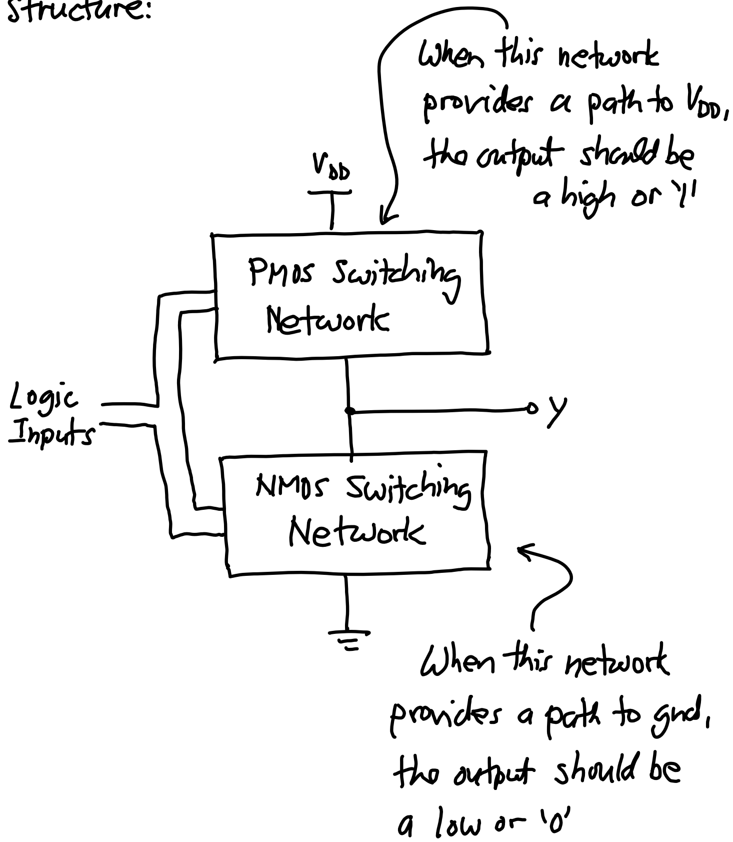
Through a similar analysis:

$$t_{pLH} = R_{on} C_L \left\{ \ln\left[\frac{4(V_{DD} - |V_{TP}|)}{V_{DD}} - 1\right] + \frac{2|V_{TP}|}{(V_{DD} - |V_{TP}|)} \right\}$$

$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

Complex CMOS Gates

To realize more complex gates, use the following structure:



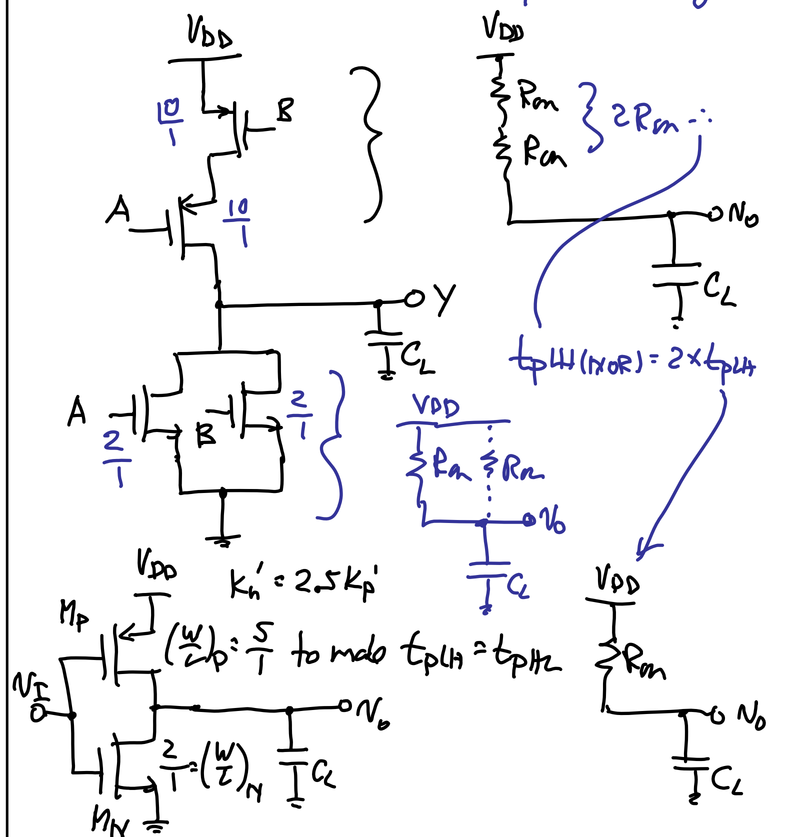
- For CMOS, to save power consumption, must avoid a conductive path connecting V_{DD} and ground in steady-state
- Otherwise, too much current will flow and dissipate power
- Should also minimize this path during transitions

CMOS NOR Gate

A	B	$Y=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

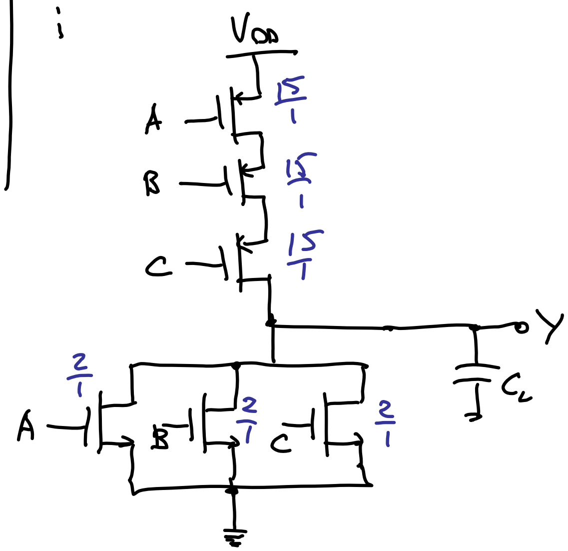
When both inputs are '0', there should be a path to V_{DD} ↳ '1'

Anytime there is a '1' in the input, need to pull down to gnd



How about 3 inputs (NOR)?

A	B	C	$Y = \overline{A+B+C}$
0	0	0	1
0	0	1	0
0	1	0	0
⋮	⋮	⋮	⋮



- What's Next?
- EE130: Semiconductor Devices
  - Did you like the physics parts? If so, then this is the course for you.
  - Will go much deeper and cover
    - Energy band diagrams
    - Short channel MOS
    - More accurate physical structure
    - Heterojunctions
    - Much more …
- EE143: Semiconductor Device Fabrication
  - Planar wafer-level fabrication methods that make IC's possible
  - Tools and chemistry
  - Process flow design
  - Hands-on wafer fabrication
- EE140: Analog Integrated Circuits
  - Supply and temperature independent biasing
  - Much larger circuits
  - Deeper understanding of op amps
  - Stability compensation
  - Feedback methods (by inspection)
- EECS151: Digital Integrated Circuits
  - Build upon propagation delay concepts
    - Short channel devices
  - Logic gates, adders, etc.
  - System-level design
    - Interconnect issues
    - Programmable arrays

- What's Next? (cont.)
- EE147: Microelectromechanical Systems (MEMS)
  - I'm biased, but … this is the coolest stuff, period!
  - Mechanics and Materials
  - Methods for fabricating tiny mechanics
  - Mechanical circuit design
  - You'll learn that all of your EE math skills and circuit techniques can just as easily be applied to mechanical devices and systems
  - Applications to sensing and RF