EE 105 **MICROELECTRONIC DEVICES & CIRCUITS** **FALL 2020**

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DETAILED COURSE SCHEDULE (TENTATIVE)

The following chart **tentatively** describes the material to be covered in the course EE 105, Microelectronic Devices & Circuits. It indicates material to be covered for each dated lecture along with the corresponding sections of the textbook "Microelectronic Circuits" by Sedra & Smith (S&S). Also indicated are the scheduling of labs and midterms and the due dates for problem sets.

Date	No.	Material to be Covered	Reading	HW Due	Laboratory
Aug. 26	1	Administrative Information	Handouts		
28	2	Introduction: Signal Types, Communication Systems	S&S: §1.1-1.3		
31	3	Review: Frequency Response, Transfer Functions, Impedance, Bode Plots	S&S: §1.6		
Sept. 2	4	Review: Amplifier Models, Input Resistance, Output Resistance	S&S: §1.4-1.5		
4	5	Review: Ideal Op Amps, Negative Feedback, Ideal Op Amp Ckts.	S&S: §2.1-2.5	HW#1	
7		*Labor Day Holiday – No Class*			
9	6	Non-ideal Op Amps: Finite Gain and Bandwidth	S&S: §2.7		
*11	7	Non-ideal Op Amps: Closed-loop Ckts. Using Finite Gain-BW Op Amps	S&S: §2.7	HW#2	
14	8	Non-ideal Op Amps: Finite R_i and R_o, Limiting, Slew Rate	S&S: §2.8		*LAB#1*
16	9	Non-ideal Op Amps: Input Offset Voltage, Input Bias Currents	S&S: §2.6		Review Passive
*18	10	Generalized Elements: Nonlinear R's, C's, and L's, Examples & Physics	S&S: §4.1-4.2	HW#3	Networks
21	11	Examples of Nonlinear Elements: Diodes, Junction Capacitors	S&S: Ch 3, §4.3-4.4		*LAB#2*
23	12	Examples of Nonlinear Elements: MOSFETs, Cut-off & Linear Operation	S&S: §5.1-5.2		Characterize
25	13	MOSFETs: Saturation Operation, Body Effect	S&S: §5.2-5.4	HW#4	741 Op Amp
28	14	BJTs: Regions of Operation, Large Signal Models, F.A. DC Analysis.	S&S: §6.1		*LAB#2*
30	15	BJTs: Cut-off, Saturation DC Analysis, IV Curves	S&S: §6.2		(cont'd)
Oct. *2	16	Parameter-Independent Biasing for BJTs, MOS Biasing	S&S: §5.3, §6.3	HW#5	
5	17	Small-Signal Analysis of General Non-Linear Ckts.			*LAB#3*
7	18	Transistors as Amplifiers, Small-Signal Modelling of (F. A.) BJTs	S&S: §7.1-7.2		Configurable
9	19	Small-Signal Modelling (cont.): BJTs, Saturated MOS Xsistors	S&S: §7.2	HW#6	Amplifiers
12	20	Small-Signal Analysis Example: Common Emitter Amplifier	S&S: §7.3-7.5		*LAB#3*
14	21	Freq. Response of Xsistor Amps.: High Frequency S.S. Models	S&S: §10.2		(cont'd)
*16	22	Determination of $C\pi$ and $C\mu$, Brute Force H.F. Solution	S&S: §10.2-10.3	HW#7	
19	23	H.F. Solution (cont.), OCTC Analysis	S&S: §10.3-10.4		*LAB#4*
21	24	OCTC Analysis C.E. Amplifier Example	S&S: §10.4		Biasing
23	25	SCTC Analysis, C.E. Amplifier Example	S&S: §10.1	HW#8	
26	26	Miller Effect, C.E. Design Project Hints	S&S: §10.3.3		*LAB#5*
28	27	Other Amplifier Configurations: C.C., C.B., Generally-Loaded Xsistor	S&S: §10.5-10.6		Analog
*30	28	Generally-Loaded Xsistor (cont.)	S&S: §7.3		Design Project
30		***Midterm Exam***			
Nov. 2	29	Inspection Analysis: C.E. w/ degen./C.C. Cascade	S&S: §7.3, 10.5-10.6		*LAB#5*
4	30	C.E. w/ degen./C.C. Cascade (cont.)	S&S: §8.3-8.4		(cont'd)
6	31	Design of Multi-Transistor Amplifiers	S&S: Ch. 9	HW#9	
9	32	Inspection Analysis: Cascode Configuration			*LAB#5*
11		*Veterans Day Holiday – No Class*	S&S: §8.5		(cont'd)
13	33	Cascode Configuration (cont.)	S&S: §8.5		
16	34	C.C. Output Drivers, Simple Current Sources	S&S: §8.2,12.1-12.2		*LAB#6*

18	35	Differential Pair, Simple Op Amp & Comparator	S&S: §9.1-9.3		Mixed Mode
20	36	Review of the CMOS Inverter: VTC	S&S: §14.1-14.3	HW#10	Design Project
23	37	Propagation Delay, Power Dissipation	S&S: §14.4, 14.6		*LAB#6*
25		*Thanksgiving Holiday – No Class*			(cont'd)
27		*Thanksgiving Holiday – No Class*			
30	38	Ring Oscillator, Current Starved Inverter			*LAB#6*
Dec. 2	39	Voltage-Controlled Ring Oscillator			(cont'd)
4	40	Driver Circuits: Distributed Wiring Capacitance, Cascaded Inverters	S&S: §14.5	HW#11	
7		*Reading/Review/Recitation (RRR) Week*			*LAB#6*
9		*Reading/Review/Recitation (RRR) Week*			(cont'd)
*11		*Reading/Review/Recitation (RRR) Week*			
17		***Final Exam Group 15: Thursday, Dec. 17, 3-6 p.m.***			

* Dates with an asterisk represent days that I cannot make the usual lecture time. On these dates I will make appropriate arrangements for the lecture. These will likely entail alternative lecture times, possibly in the evenings, but since this course will be recorded, you can always watch the recording if you cannot attend the live lecture.