PROBLEM SET #6

Issued: Friday, October 2nd, 2020

Due: Friday, October 9th, 2020, at 12:00 noon via Gradescope.

Reading Assignment: Sedra & Smith, §6.1–6.3, §5.3

1. As discussed in lecture, when a pn junction is forward-biased, the depletion region decreases in width and the potential barrier blocking diffusion of majority carriers is lowered. This results in majority carriers (holes in *p*-type semiconductors and electrons in *n*-type) diffusing across the depletion region, at which point they become minority carriers. This phenomenon is called minority-carrier injection. This injection forms an excess of minority carriers at the edges of the depletion region which increases the equilibrium concentrations of minority carriers, n_{P0} and p_{N0} by a factor of $e^{\frac{qV_f}{kT}}$, where V_f is the applied forward bias voltage and at room temperature $\frac{kT}{q} = V_T = 25.9$ mV.

(a) If the total forward current in the pn junction under forward bias is given by

$$I_f = I_s\left(e^{V_f/V_T} - 1\right) = \left(J_p^{\text{diff}} + J_n^{\text{diff}}\right) \cdot A$$

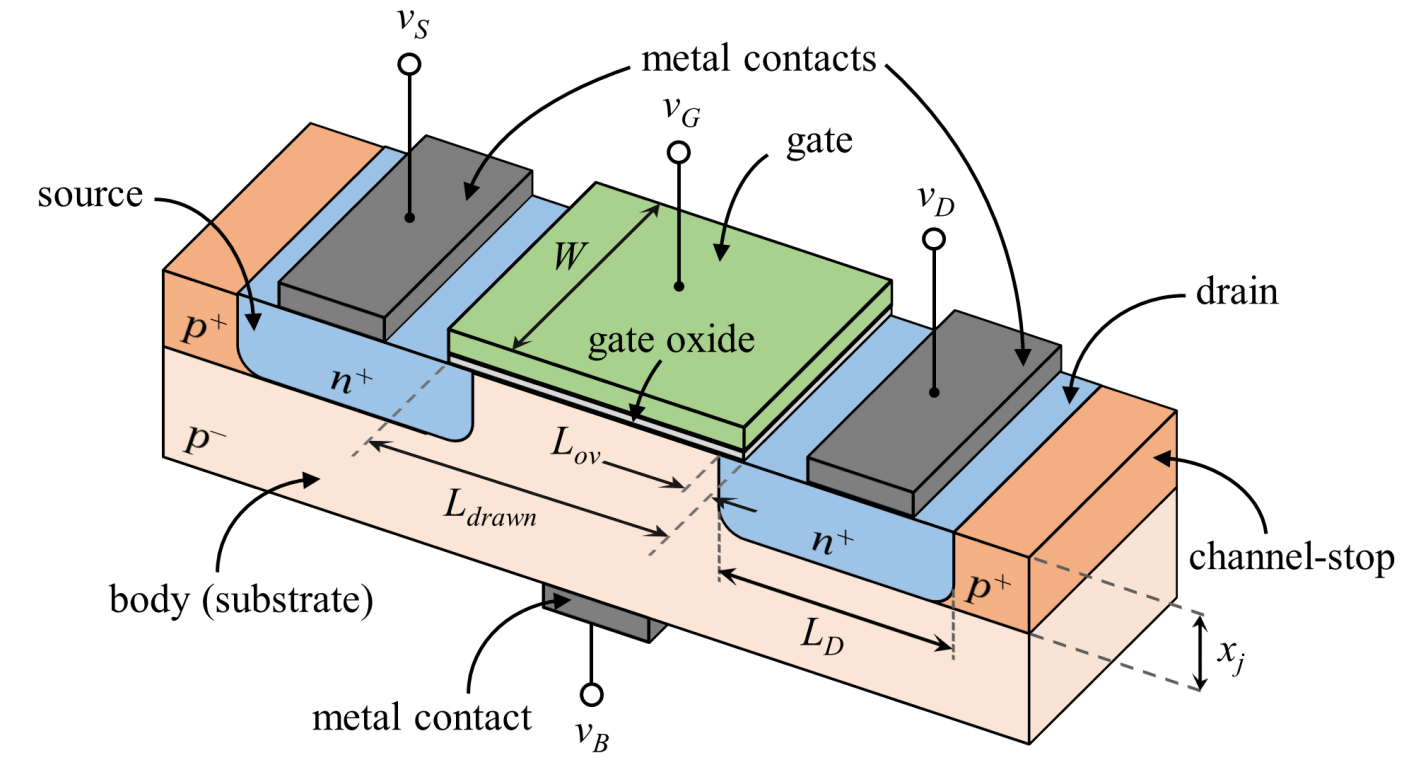
derive expressions for the hole diffusion current density J_p^{diff}, electron diffusion current density J_n^{diff}, and saturation current I_s. These expressions should be in terms of q, the intrinsic carrier concentration n_i, the cross-sectional area A, the diffusion constants D_p & D_n, the doping concentrations N_A & N_D, the coordinates for the outer edges of the pn junction $-w_p$ & w_n, and the coordinates for the edges of the depletion region $-x_p$ & x_n. You may assume diffusion lengths much longer than $(w_p - x_p)$ and $(w_n - x_n)$, i.e. you can assume a linear concentration distribution within the semiconductors.

(b) If the pn junction has cross-sectional area $A = 100\ \mu\text{m}^2$; total length $L = w_n + w_p = 2\ \mu$m; doping $N_A = 10^{19}\ \text{cm}^{-3}$ & $N_D = 10^{16}\ \text{cm}^{-3}$; $n_i = 1.5 \times 10^{10}\text{cm}^{-3}$; and diffusion constants $D_p = 12\ \text{cm}^2/\text{sec}$ & $D_n = 36\ \text{cm}^2/\text{sec}$, calculate I_S. Assume that the *p*-type and *n*-type semiconductors have equal widths (i.e., $w_p = w_n$).

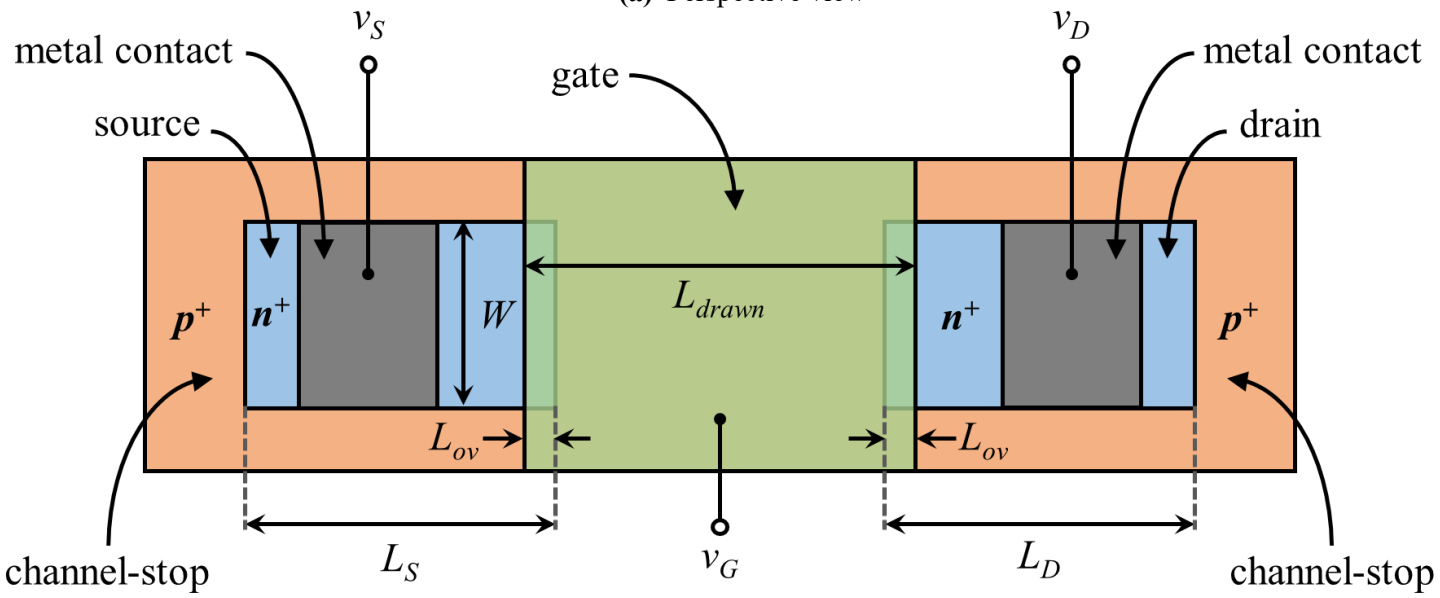
(c) If a forward voltage $V_f = 750$ mV is applied across this junction, find the resulting hole and electron diffusion current densities J_p^{diff} and J_n^{diff}. What is the total forward current?

2. This question will examine a traditional MOSFET and the parasitic capacitances inherent in its design. Figure PS6.1 below presents both (a) a perspective view and (b) a top view of an NMOS transistor with relevant dimensions labeled. The four parasitic capacitances between terminals of the MOSFET are named with the subscripts denoting the terminals that each internal capacitance appears between (e.g. C_{gs} refers to the gate-to-source capacitance).

Note that the source and drain regions do not stop right at the edges of the gate, but rather they extend underneath the gate by a distance L_{ov}. This overlap between the gate and the source/drain regions is due to diffusion of the dopants used to create the source and drain.



(a) Perspective view



(b) Top view

Figure PS6.1

PARAMETER	*VALUE*	*UNIT*
W	10	μm
L_{drawn}	2	μm
L_{ov}	0.025	μm
L_D	20	μm
L_S	20	μm
t_{ox}	5	nm
x_j	0.1	μm
$N_{D,source}$	10^{19}	cm^{-3}
$N_{D,drain}$	10^{19}	cm^{-3}
N_B	10^{16}	cm^{-3}
N_{CS}	10^{18}	cm^{-3}
n_i	1.5×10^{10}	cm^{-3}
V_T	25.9	mV
ϵ_o	8.85×10^{-12}	F/m
$\epsilon_{r,Si}$	11.7	–
$\epsilon_{r,SiO2}$	3.9	–
v_G	3	V
v_D	1	V
v_S	0	V
v_B	-1	V

Table PS6.1

(a) First, examine the capacitance resulting from the overlap between the gate and the source and drain regions. Referring to the MOSFET in Fig. PS6.1 and the parameters in Table PS6.1, find an expression and a numerical value for C_{ov}, the overlap capacitance between the gate and the source (or drain) region. (Hint: You may want to start by defining and solving for the gate capacitance per unit area, C_{ox}''.)

(b) In addition to the overlap capacitance, the gate and the silicon substrate form a capacitor with the gate oxide (and any depletion region in the substrate) serving as a dielectric. Assuming the MOSFET is biased in the linear region of operation, find an expression and a numerical value for the gate-to-substrate capacitance $C_{gate\text{-}sub}$. In the linear region, by convention we usually assume this capacitance is split evenly between the total gate-to-

source capacitance C_{gs} and total gate-to-drain capacitance C_{gd}. Taking into account your result from (a), find expressions and values for C_{gs} and C_{gd}.

(c) The other two parasitic capacitances, C_{db} and C_{sb} are depletion capacitances that arise from the reverse-biased pn junctions between the drain and body and the source and body, respectively.

Before finding the values of C_{db} and C_{sb}, you must first find the zero-bias junction capacitances by considering the geometry of the pn junction for the source and drain regions. As shown in Fig. PS6.1, the p-type silicon surrounding the source and drain regions has two different levels of doping. The silicon below the source and drain regions is lightly doped (p^-) with bulk doping concentration N_B, while the silicon surrounding the outer perimeters of the source and drain is heavily doped (p^+) with channel-stop doping concentration N_{CS}. This heavily doped channel-stop is created using ion implantation and its job is to prevent unwanted inversion in the field regions between transistors.

First find an expression and value for C_{j0}, the zero-bias junction capacitance per unit area for the bottom surface of the source and drain regions. Then find an expression and value for C_{jsw0}, the zero-bias junction capacitance per unit length for the sidewalls of the source and drain regions. (Hint: These junction capacitances are of the same form as the junction capacitance for a zero-bias pn junction derived in lecture, with the slight modification that C_{j0} is per unit area and C_{jsw0} is per unit length.)

(d) Using C_{j0} and C_{jsw0} and the dimensions given in Fig. PS6.1 and Table PS6.1, find expressions and values for the total zero-bias drain-body and source-body capacitances C_{db0} and C_{sb0}.

(e) Now, using the model for the depletion capacitance of a reverse-biased pn junction given in lecture, find expressions and numerical values for the total drain-body and source-body capacitances C_{db} and C_{sb}.

(f) Sketch all four capacitors, C_{gs}, C_{gd}, C_{db} and C_{sb} in their correct locations on a cross-sectional view of the MOSFET. Additionally, sketch the depletion regions that form the junction capacitances with regions of fixed and free charge labeled. Make sure to qualitatively include the effects of uneven doping (i.e., $N_A \neq N_D$) in your drawing. Which region of operation is this MOSFET in?

3. Identify the region of operation of an NMOS transistor with $K_n = 250\ \mu A/V^2$ and $V_{tn} = 1\ V$ for the following bias voltages. You may assume that the transistors are symmetric with respect to their source and drain regions.

(a) $V_{GS} = 5$ V and $V_{DS} = 6$ V

(b) $V_{GS} = 0$ V and $V_{DS} = 6$ V

(c) $V_{GS} = 2$ V and $V_{DS} = 2$ V

(d) $V_{GS} = 2$ V and $V_{DS} = -0.5$ V

(e) $V_{GS} = 3$ V and $V_{DS} = -6$ V

(f) $V_{GS} = -2$ V and $V_{DS} = -1$ V