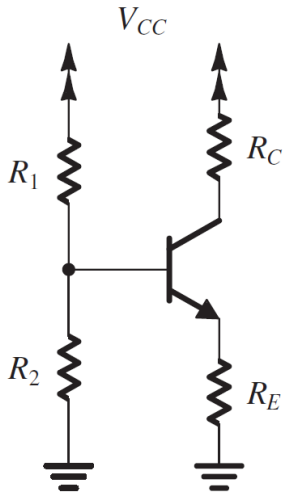
***5.42** Various NMOS and PMOS transistors, numbered 1 to 4, are measured in operation, as shown in the table at the bottom of the page. For each transistor, find the values of $\mu C_{ox} W/L$ and V_t that apply and complete the table, with V in volts, I in μA, and $\mu C_{ox} W/L$ in μA/V^2. Assume $\lambda = 0$.

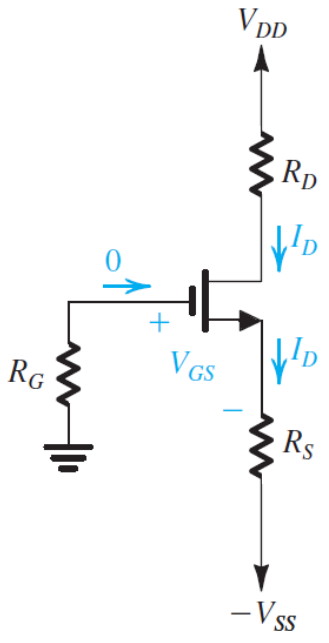
Case	Transistor	V_S	V_G	V_D	I_D	Type	Mode	$\mu C_{ox} W/L$	V_t
a	1	0	1	2.5	100				
	1	0	1.5	2.5	400				
b	2	5	3	−4.5	50				
	2	5	2	−0.5	450				
c	3	5	3	4	200				
	3	5	2	0	800				
d	4	−2	0	0	72				
	4	−4	0	−3	270				

D 7.106 Consider the single-supply bias network shown in Fig. 7.52(a). Provide a design using a 9-V supply in which the supply voltage is equally split between R_C, V_{CE}, and R_E with a collector current of 0.6 mA. The transistor β is specified to have a minimum value of 90. Use a voltage-divider current of $I_E/10$, or slightly higher. Since a reasonable design should operate for the best transistors for which β is very high, do your initial design with $\beta = \infty$. Then choose suitable 5% resistors (see Appendix J), making the choice in a way that will result in a V_{BB} that is slightly higher than the ideal value. Specify the values you have chosen for R_E, R_C, R_1, and R_2. Now, find V_B, V_E, V_C, and I_C for your final design using $\beta = 90$.



(a)

D 7.93 Using the circuit topology displayed in Fig. 7.48(e), arrange to bias the NMOS transistor at $I_D = 0.5$ mA with V_D midway between cutoff and the beginning of triode operation. The available supplies are ±5 V. For the NMOS transistor, $V_t = 1.0$ V, $\lambda = 0$, and $k_n = 1$ mA/V^2. Use a gate-bias resistor of 10 MΩ. Specify R_S and R_D to two significant digits.



(e)

D ***7.26** An NMOS amplifier is to be designed to provide a 0.20-V peak output signal across a 20-kΩ load that can be used as a drain resistor. If a gain of at least 10 V/V is needed, what g_m is required? Using a dc supply of 1.8 V, what values of I_D and V_{OV} would you choose? What W/L ratio is required if $\mu_n C_{ox} = 200\ \mu A/V^2$? If $V_t = 0.4$ V, find V_{GS}.

***7.33** Figure P7.33 shows a discrete-circuit amplifier. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite). All capacitors behave as short circuits for signals and as open circuits for dc.

(a) If the transistor has $V_t = 1$ V, and $k_n = 4\ mA/V^2$, verify that the bias circuit establishes $V_{GS} = 1.5$ V, $I_D = 0.5$ mA, and $V_D = +7.0$ V. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.

(b) Find g_m and r_o if $V_A = 100$ V.

(c) Draw a complete small-signal equivalent circuit for the amplifier, assuming all capacitors behave as short circuits at signal frequencies.

(d) Find R_{in}, v_{gs}/v_{sig}, v_o/v_{gs}, and v_o/v_{sig}.

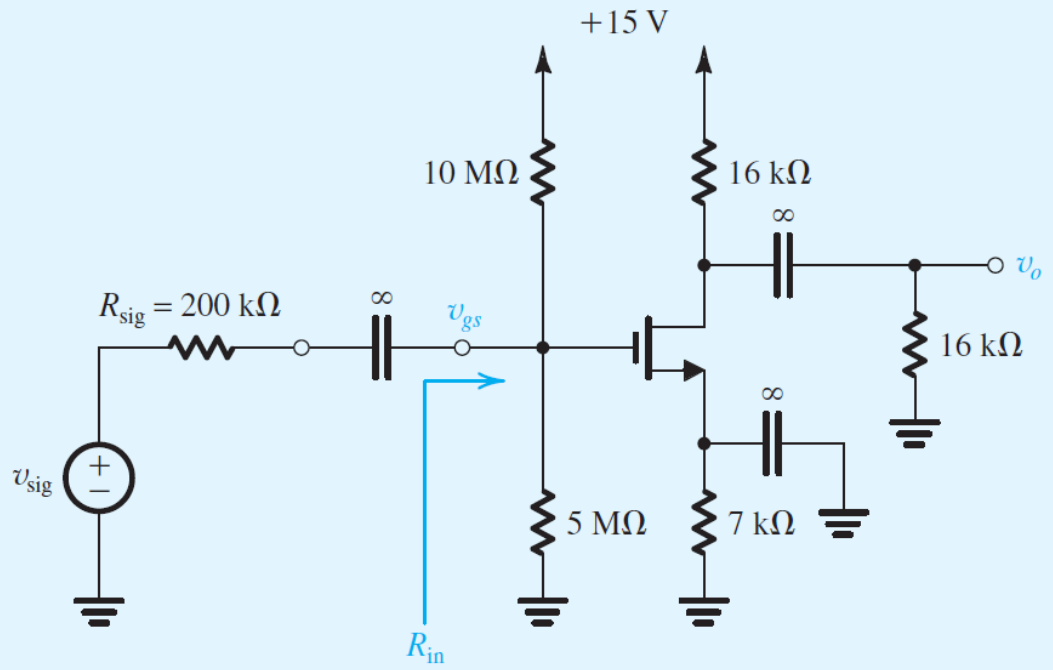


Figure P7.33