Laboratory 3: Configurable Amplifiers Using Small-Signal MOS Resistors

Preliminary Exercises

This lab focuses on the use of MOS transistors as voltage-controlled variable resistors. In the lab, we will specifically demonstrate a gain-controllable (i.e., configurable) inverting amplifier and a bandwidth-controllable lowpass filter using op amps, resistors, capacitors, and a discrete MOS transistor.

The preliminary exercises in this section aim to prepare you for this lab. In completing these exercises, you should assume an NMOS transistor with the following parameters:

Transconductance Parameter, $K_n=\mu_n C_{ox}(W/L)$:	451.9 μA/V^2
Nominal Threshold Voltage, V_{t0}:	1.4 V
Surface Potential, $2\phi_f$:	0.66V
Body Effect Parameter, γ:	0.49V$^{1/2}$

Other device parameters can be found in the 'cd4007ub.mod' file online, which is a SPICE model.

1. Gain-Controllable Amplifier

(a) For the MOS transistor circuit shown in Fig. PL3.1(a) below, calculate and tabulate (using the *Results Sheet for Preliminary Exercises*) the values of the small-signal resistance R_{MOS} from drain to source for values of control voltage V_C ranging from 0V to 10V, in steps of 1V. Then, plot your values of R_{MOS} versus V_C on a graph. Again, assume the MOS device parameters given at the beginning of this pre-lab.

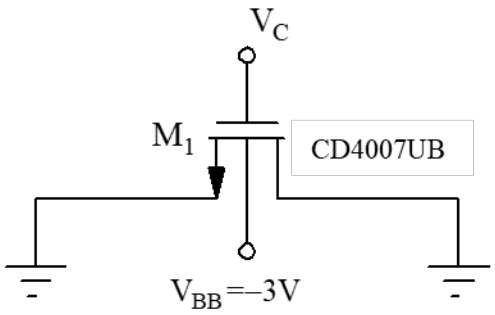

Figure PL3.1(a)

(b) For the inverting amplifier circuit shown in Fig. PL3.1(b) (which uses an op amp defined by 'lmc6482.mod' and an MOS transistor with parameters as in the beginning of this pre-lab defined by 'cd4007ub.mod'), calculate and tabulate (using the *Results Sheet for Preliminary Exercises*) the gain V_o/V_i of this amplifier for values of control voltage V_C ranging from 0V to 10V, in steps of 1V. Then, plot the gain versus V_C on a graph. (Hint: Be careful when determining gain at V_C=0V)

Assume for this pre-lab that the MOS transistors have zero leakage currents.

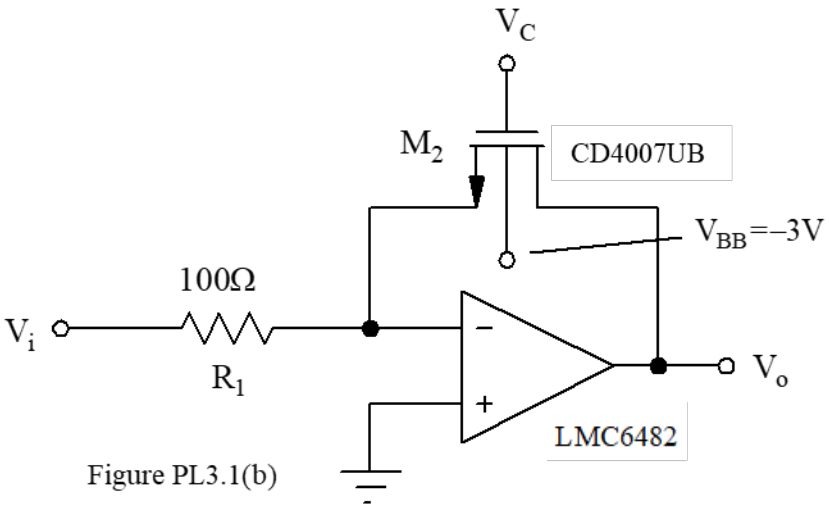

Figure PL3.1(b)

(c) Calculate and tabulate (using the *Results Sheet for Preliminary Exercises*) the 3-dB bandwidth of the amplifier for values of V_C ranging from 2V to 10V, in steps of 1V. Use SPICE to generate Bode plots for this amplifier, for values of V_C ranging from 1V to 10V. (Plot all curves on the same graph.)

2. Bandwidth-Controlled (Unity-Gain) Filter

(a) For the filter circuit shown in Fig. PL3.2(a), the op amp uses the model given in 'lmc6482.mod', and the MOS transistors M_1 and M_2 use the model given at the beginning of this pre-lab and in 'cd4007ub.mod'. Assuming for now that M_1 and M_2 are identical, calculate and tabulate (using the *Results Sheet for Preliminary Exercises*) the 3dB bandwidth of the filter for values of control voltage V_C from 2V to 10V, in steps of 1V.

(b) Using SPICE, generate Bode plots (all on the same graph) for the circuit of Fig. PL3.2(a) for values of V_C from 2V to 10V, in steps of 1V. Use the SPICE model 'cd4007ub.mod' for each NMOS transistor and use the model in 'lmc6482.mod' for the op amp.

(c) Suppose that due to fabrication mismatches, the channel length of M_1 was 10% larger than that of M_2 (everything else remains identical). What then is the passband gain of this filter?

(d) Suppose that due to fabrication mismatches, the nominal threshold voltage V_{t0} of M_1 was 20% larger than that of M_2 (everything else remains identical). Calculate and tabulate (using the *Results Sheet for Preliminary Exercises*) the gain V_o/V_i of the filter for control voltage V_C values from 2V to 10V, in steps of 1V. Plot the gain V_o/V_i versus V_C on a graph.

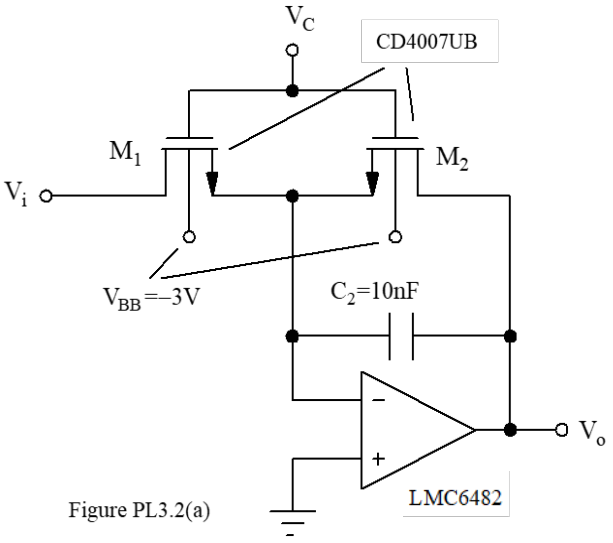

Figure PL3.2(a)

Helpful Hints for SPICE Simulation

Some notes on creating a MOSFET instance for this lab:

(1) For the NMOS transistor, you should use the model file on the course website, 'cd4007.mod'.

(2) To use an NMOS transistor in your netlist, you must first include the model file using a .include statement:

```
.include <path_to_model_file>
```

(3) Then, to create an instance of the MOSFET use the following code:

```
M<name> <drain> <gate> <source> <body> <model_name> (W=<value> L=<value>)
```

Replace `<name>` with the desired name of your NMOS instance and `<model_name>` with the name of the NMOS model, which is defined within 'cd4007.mod'. For the CD4007UB the W is 42 µm and L is 10 µm.

(4) To run a nested DC sweep (i.e., to sweep two sources in the same simulation), the syntax is very similar to the standard DC sweep:

```
.dc <source1> <start1> <stop1> <step1> <source2> <start2> <stop2> <step2>
```

Note that in this analysis, `<source1>` is swept while `<source2>` is stepped.

(5) To run a nested AC sweep (i.e., to step a DC source while running ac sweeps for each step), the syntax is very similar to the standard AC sweep:

```
.ac <LIN|DEC|OCT> <number of samples> <fstart> <fstop> SWEEP <source> <start> <stop> <step>
```

Replace `<source>` with the name of an independent voltage source and use `<start>`, `<stop>` and `<step>` to set the starting voltage, final voltage and voltage step, respectively.

Laboratory 3: Configurable Amplifiers Using Small-Signal MOS Resistors
Results Sheet for Preliminary Exercises

1. Gain-Controllable Amplifier

Table PLR3.1. Gain-Controllable Amplifier Characteristics

V_C [V]	(a) R_{MOS}	(b) Gain, V_o/V_i	(c) 3dB Bandwidth
0			
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			

Attach the necessary annotated plots for parts (a), (b), and (c).

2. Bandwidth-Controlled (Unity-Gain) Filter

Table PLR3.2. Bandwidth-Controllable Amplifier Characteristics

V_C [V]	(a) 3dB Bandwidth	(d) Gain, V_o/V_i
2		
3		
4		
5		
6		
7		
8		
9		
10		

(a) Fill in the table above.

(b) Attach annotated SPICE plot.

(c) Gain, V_o/V_i = _____

(d) Fill in the table above and attach the necessary annotated plot.