



EECS 105 – Microelectronic Devices and Circuits

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Dept. EECS,
UC Berkeley

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Course Web Site <http://www-inst.EECS.Berkeley.EDU/~ee105/>

Homework Assignment # 11, Due April 13, 2001

11.1 Common-Source Amplifier with Current Source Supply & SPICE Simulation

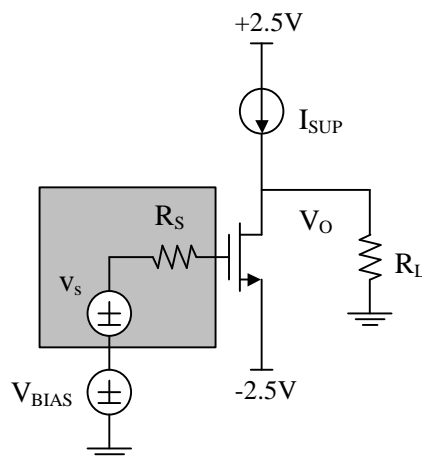
Design a common-source amplifier with a current source supply as shown in the figure below. The NMOS channel length is $L=2\mu\text{m}$ and the substrate is tied to -2.5V . V_{BIAS} is set such that $V_{\text{O}}=0\text{V}$

(1) Choose V_{BIAS} , W and I_{SUP} so that the amplifier has an overall voltage gain of -100 when $R_{\text{L}} \rightarrow \infty$ and the amplifier has an overall voltage gain of -20 when $R_{\text{L}} = 20\text{k}\Omega$.

(2) Verify your result using SPICE. You should use Level 1 MOSFET model and specify the proper model parameters in your simulation. Fill the table with your simulation results. Does the simulation match your hand analysis? What are the reasons if they don't match?

	Desired	Simulated
V_{O}	0V	
Voltage gain A_v ($R_{\text{L}} \rightarrow \infty$)	-100	
Voltage gain A_v ($R_{\text{L}} = 20\text{k}\Omega$)	-20	

(3) Bias the amplifier so that $V_{\text{O}}=0\text{V}$ (in case V_{O} is not equal to 0V in part(2)), apply a sinusoidal signal v_s to the amplifier and ramp v_s up to get rail to rail output, at what value of v_s (the amplitude) do you see the output waveform distorts and clips? What is the peak-to-peak output swing when the distortion appears?



Device Data

$$V_{\text{Tn}} = 0.7\text{V}$$

$$\mu_{\text{n}}C_{\text{ox}} = 50\mu\text{A}/\text{V}^2$$

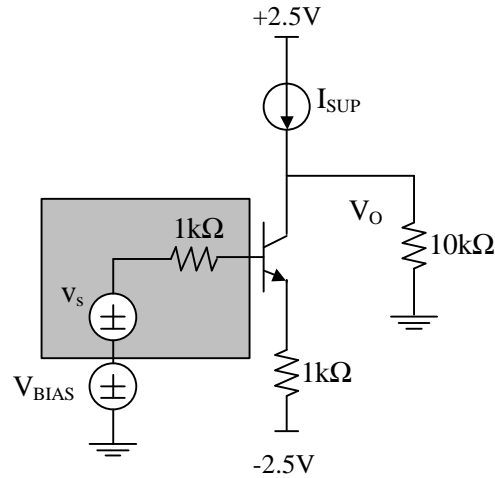
$$\lambda_{\text{n}} = 0.05\text{V}^{-1}$$

$$r_{\text{oc}} \rightarrow \infty$$

11.2 Common-Emitter Amplifier with Emitter Degeneration

Given an NPN common-emitter amplifier with emitter degeneration resistor as shown in the figure

- (1) Find the value of V_{BIAS} so that $V_O=0V$ when $I_{SUP}=200\mu A$
- (2) Calculate the two-port parameters R_{in} and R_{out}
- (3) Calculate the overall transconductance
- (4) Calculate the overall voltage gain



Device Data

$$I_s = 10^{-15} A$$

$$\beta_F = 100$$

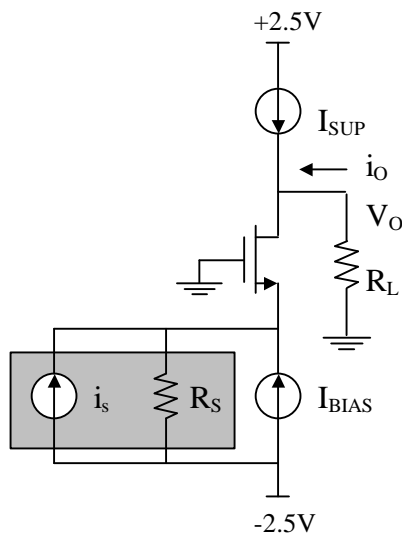
$$V_A = 25V$$

$$r_{oc} \rightarrow \infty$$

11.3 Common-Gate Amplifier

Given an NMOS common-gate amplifier with a current source supply as shown in the figure (The bulk node of the NMOS transistor is tied to its source)

- (1) Find the value for I_{BIAS} so that $V_O=0V$ when $I_{SUP}=100\mu A$ (you can neglect R_S)
- (2) Calculate the two-port parameters R_{in} and R_{out}
- (3) Calculate the overall current gain
- (4) Calculate the overall transresistance



Device Data

$$W/L=4/2$$

$$V_{Th} = 0.7V$$

$$\mu_n C_{ox} = 50\mu A/V^2$$

$$\lambda_n = 0.05V^{-1}$$

$$r_{oc} \rightarrow \infty$$

$$R_L = 10k\Omega$$

$$R_S = 10k\Omega$$