EECS 105 – Microelectronic Devices and Circuits

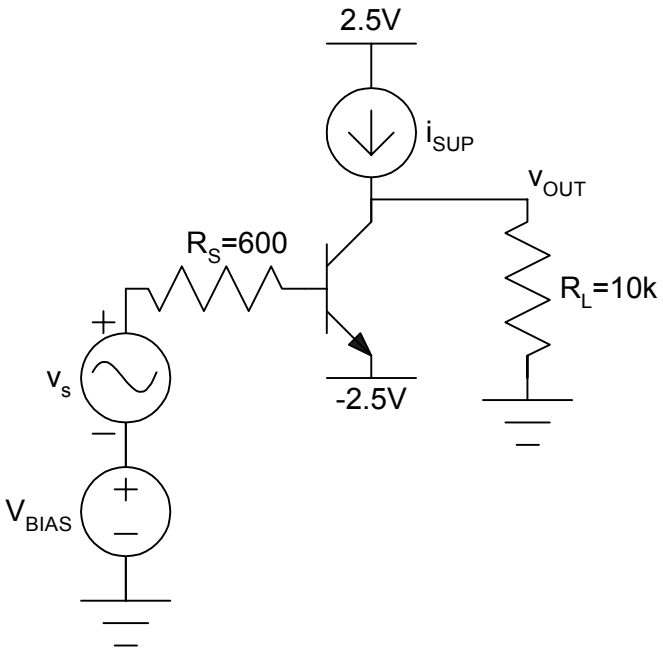
Spring 2001, Prof. A. R. Neureuther
Dept. EECS, 510 Cory 642-4590
UC Berkeley Office Hours M11, (Tu2), W2, Th2, F11
Course Web Site http://www-inst.EECS.Berkeley.EDU/~ee105/

Homework Assignment # 13, Due April 27, 2001

Use the following parameters for all BJT devices.

NPN	PNP
β=100	β=50
$V_{CE\text{-}SAT}$=0.1V	$V_{EC\text{-}SAT}$=0.1V
V_{BE}=0.7V	V_{EB}=0.7V
V_A=20V	V_A=25V
W_B=1μm	W_B=1μm
$N_{ED}=10^{19}/cm^3$	$N_{EA}=10^{19}/cm^3$
$N_{BA}=5x10^{17}/cm^3$	$N_{BD}=5x10^{17}/cm^3$
$N_{CD}=10^{16}/cm^3$	$N_{CA}=10^{16}/cm^3$

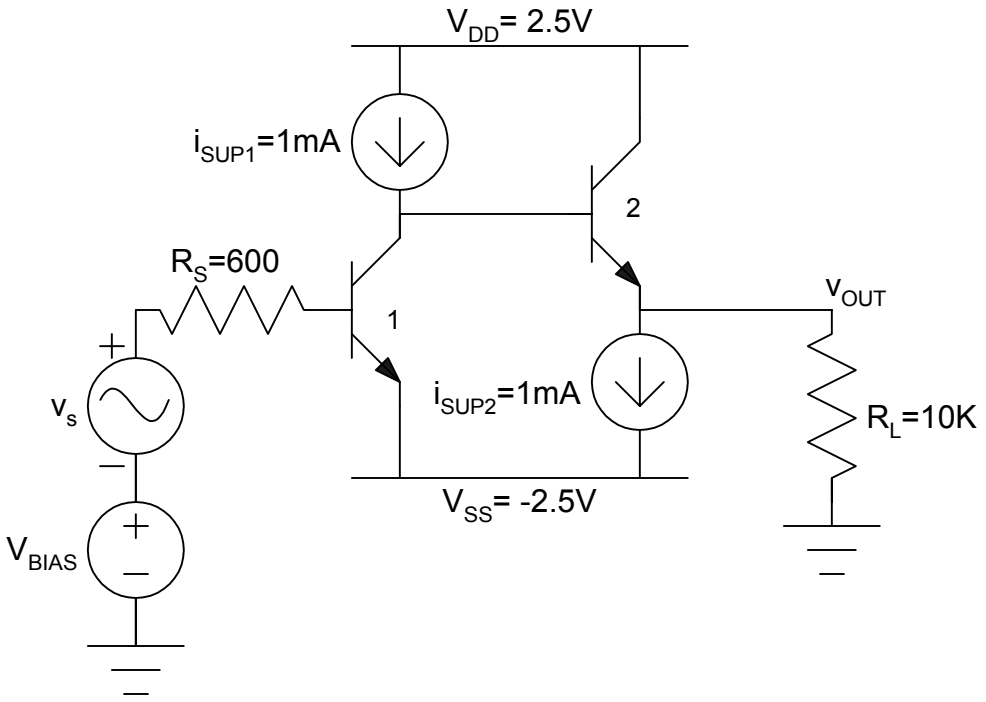
13.1) **Common Emitter Design**
Consider the following circuit:



Find I_{SUP}, V_{BIAS} and A, the area of the base, such that the following constraints are met:

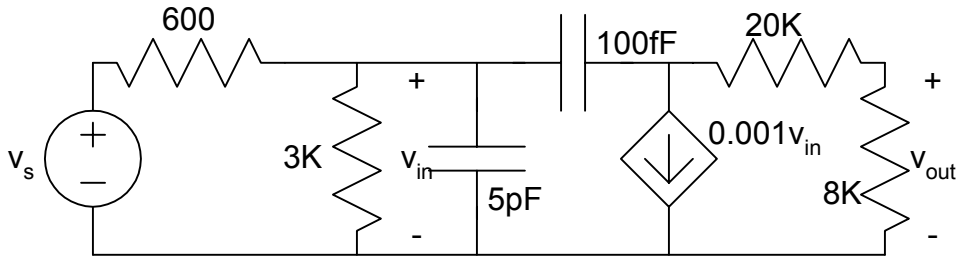
V_{OUT}=0V
$r_{oc}=r_o$
Overall voltage gain of at least 75 at low frequencies
Lowest frequency pole at 50MHz or higher (the only capacitor you should consider is C_π)
Minimize the large signal power dissipation

13.2) **Multistage Frequency Response with Open-Circuit Time Constants**
Consider the following circuit:



Assuming that V_{OUT}=0, r_{oc1}=r_{o1}, r_{oc2}=r_{o2}, and the area of each base is 10μm x 10μm, find this circuit's lowest frequency pole and its –3dB frequency, both in Hz. You should consider the effect of C_π and C_μ but not the capacitance to the substrate.

13.3) **Miller Approximation**
Find the lowest frequency pole for each of the following circuits.
a)



b)