EECS 105 - Microelectronic Devices and Circuits

Homework Assignment \# 2, Due February 2, 2001
All circuits in the following problems are fabricated in a N -well CMOS process
oxide mask (dark field)
polysilicon mask (clear field)
contact mask (dark field)
0 metal mask (clear field)
N-well mask (dark field)
2.1 CMOS process flow. Consider the layout of a CMOS inverter. Use the 6 step process flow in Chapter 2 and add one additional mask ( N -well) and two additional steps ( N -well implant prior to step 1 and P type source/drain implant prior to step 5.

a) Draw the cross section at cut-line A-A immediately after polysilicon etching
b) Draw the cross section at cut-line A-A immediately after contact opening

Specify substrate type, doping types in source/drain areas and each layer in your schematic.
2.2 CMOS Circuit. Consider the layout of a CMOS circuit


Draw the circuit diagram (show all wirings and MOSFETs)
2.3 IC resistors. Consider the layout of an IC resistor. Assume sheet resistances of N+ doping, polysilicon and metal are $100 \Omega$ /square, $10 \Omega /$ square and $0.01 \Omega /$ square, respectively.

a) Sketch the cross section of the resistor at cut-line A-A
b) Calculate the total resistance $\mathrm{R}_{\mathrm{BC}}$ (Contact and corner resistances should be considered in your calculation. Assume that the contact regions each contribute 0.65 squares)

### 2.4 IC resistors.

a) If the $\mathrm{N}+$ doping in problem 2.3 is 0.5 um deep and the distribution of dopant is uniform, find the doping concentration. (Assume the grid show on the drawing have 0.5 um openings)
b) A $10 \mathrm{k} \Omega$ resistor $R_{1}$ and a $5 \mathrm{k} \Omega$ resistor $R_{2}$ combines in series so that their resistances add. If $R_{1}$ has an uncertainty of $500 \Omega$ and the uncertainty in $\mathrm{R}_{2}$ is $400 \Omega$. What is the uncertainty in $\mathrm{R}_{1}+\mathrm{R}_{2}$ ?

