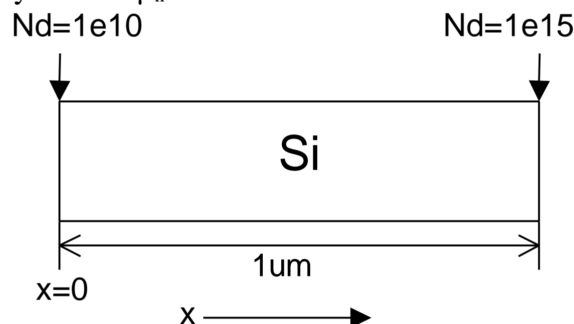
EECS 105 – Microelectronic Devices and Circuits

Spring 2001, Prof. A. R. Neureuther
Dept. EECS, 510 Cory 642-4590
UC Berkeley Office Hours M11, (Tu2), W2, Th2, F11
Course Web Site http://www-inst.EECS.Berkeley.EDU/~ee105/

Homework Assignment # 3, Due February 9, 2001

Assume room temperature for all problems

3.1) **Equilibrium current components.** A 1-micron long block of silicon is doped with donors with a linearly increasing density from 1e10 atoms/cm^3 to 1e15 atoms/cm^3. There are no acceptors. As shown in figure 2.8 on page 36 of H&S the electron mobility increases only slightly as dopant concentration decreases from 1e15 atoms/cm^3, therefore in this problem you may assume μ_n=1400cm^2/Vs for all donor concentrations.



a) Find the diffusion current density in the block, assuming that all donated electrons are still distributed the same as the dopant atoms.
b) Determine the magnitude and direction of an electric field that will exactly cancel out the diffusion current at x=0.5um.
c) Find the total current at x=0 given the field from part b.
d) Find the total current at x=1um given the field from part b.

3.2) **One-sided pn junction.** Consider a one-sided pn junction with p-side doping of N_a=1e16 atoms/cm^3 and n-side doping of N_d=5e19 atoms/cm^3. A maximum magnitude of electric field of E_{max}=5e5 V/cm can exist in the device without damaging the silicon lattice.

a) Determine the maximum depletion width that can exist in the device without damaging the silicon lattice.
b) Determine the bias voltage what would need to be applied to cause the depletion region described in part a.
c) Determine the how many times larger the depletion region described in part a is in comparison to the depletion width with no applied voltage.

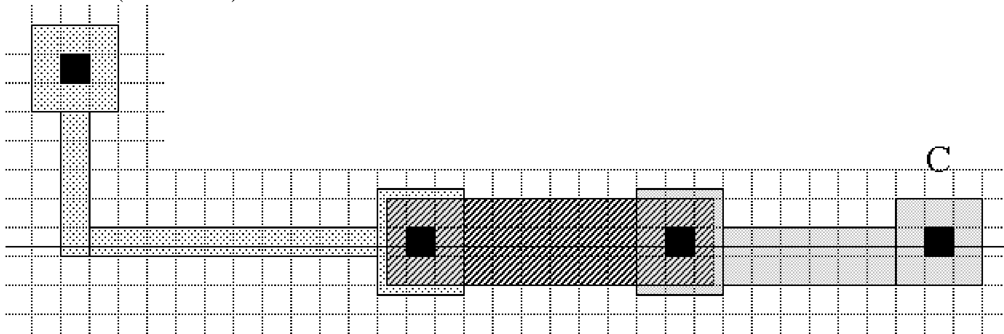
3.3) **Threshold voltage.** Consider the MOS device shown in figure 3.30 on page 153 of H&S. The gate oxide is 50nm, the p-type region is doped with N_a=1e16 atoms/cm^3, and V_{GB}=1V. You do not have to include the metal contacts on your plots.

a) Plot the charge density in the device and clearly label all important values.

b) Plot the electric field in the device and clearly label all important values.
c) Plot the potential in the device and clearly label all important values.
d) Determine if increasing the doping by a factor of 10 or increasing the gate oxide thickness by a factor of 2 will produce a larger change in the threshold voltage.

3.4) **Parasitic capacitances.** Consider the layout shown below. The oxide, polysilicon and metal layers are each 1um thick. The active regions are uniformly doped with N_d=1e17 atoms/cm^3 to a depth of 1um. The substrate was doped with N_a=1e15 atoms/cm^3. The polysilicon is doped with N_d=1e19 atoms/cm^3. Each square in the layout represents 1um^2. You may ignore the fractional squares near the middle contacts. The substrate is connected to ground and the end contacts are connected to 5V.

- oxide mask (dark field)
- polysilicon mask (clear field)
- contact mask (dark field)
- metal mask (clear field)



a) Determine the capacitance per unit area between the polysilicon and the substrate and then find the total polysilicon to substrate capacitance.
b) Determine the capacitance per unit area between the metal and the substrate and then find the total metal to substrate capacitance.
c) Determine the capacitance per unit area between the active region and the substrate and then find the total active region to substrate capacitance.