EECS 105 – Microelectronic Devices and Circuits

Spring 2001, **Prof. A. R. Neureuther**
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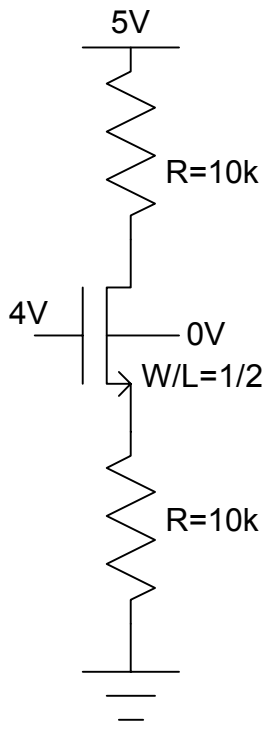
Homework Assignment # 5, Due *Wednesday* February 21, 2001

This is a shortened homework due to Presidents Day and Wednesday due date.

Use the following parameters for all MOSFET devices.

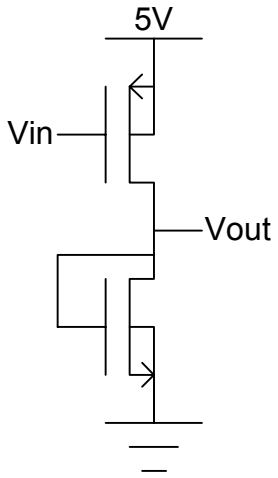
NMOS	PMOS
$\mu_n C_{ox}=50\mu A/V^2$	$\mu_p C_{ox}=25\mu A/V^2$
$V_{T0n}=1.0V$	$V_{T0p}=-1.0V$
$\gamma_n=0.6V^{1/2}$	$\gamma_p=0.6V^{1/2}$
$\lambda_n=(0.1/L)V^{-1}$ L in μm	$\lambda_p=(0.1/L)V^{-1}$ L in μm
$\phi_p=-0.42$	$\phi_n=0.42$

5.1) **Body effect and channel length modulation of MOS transistors.**
Consider the following circuit:



a) Find the width of the transistor that will cause it to be at the transition between triode and saturation. Be sure to include the body effect.
b) With the width found in part a, determine the source to drain current.
c) If the width of the transistor is doubled from part a (but W/L ratio remains constant), what region of operation will the transistor be in? Your argument should be symbolic – don't calculate any values.
d) Double the width you found in part a and then find the new source to drain current. This equation is messy – you probably want to iteratively solve for it, using your answer from part b as an initial guess.
e) Draw the small signal equivalent for the double width version of this circuit and label all components. Consider the 4 volts on the gate to be the DC component of a source that also has a small signal AC component, Vsmall. You do not need to include any of the small signal capacitances.

5.2) **CMOS amplifier.**
Consider the following circuit with PMOS sizing of 46um/10um and NMOS sizing of 42um/10um:



a) Considering only the PMOS transistor in isolation, plot current in the PMOS device (source to drain) versus Vout for Vin = 2 volts and label important values. Limit Vout to values that place the PMOS transistor into saturation.
b) Considering only the NMOS transistor in isolation, plot current in the NMOS device (drain to source) versus Vout and label important values. Limit Vout to values that keep the NMOS transistor out of cutoff.
c) Considering the whole circuit, find Vout when Vin=2 volts.
d) Draw and label the small-signal circuit for this bias point and find the voltage gain. Consider Vin to have a small signal component. You do not need to include any of the small signal capacitances.