Lecture 15: MOS Transistor models: 
Body effects, SPICE models

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Context

In the last lecture, we discussed the modes of operation of a MOS FET:
- Voltage controlled resistor model
- I-V curve (Square-Law Model)
- Saturation model

In this lecture, we will:
- add a correction due to the changing depletion region, called the body effect
- Produce small signal models for the FET
- and look at how MOS Transistors are modeled in SPICE
**Reading**

- Today, and Friday we will finish the material from chapter 4.
- Then we look at the analog characteristics of simple digital devices, 5.2→5.4
- And following the midterm, we will cover PN diodes again in forward bias, and develop small signal models: Chapter 6
- We will then take a week on bipolar junction transistor (BJT): Chapter 7
- Then go on to design of transistor amplifiers: chapter 8

**MOS operation**

- An inversion mode MOS transistor operates by producing a sheet carriers just under the oxide
- The names source and drain are picked so that the inversion charge is larger at the source end
- Approximate inversion charge $Q_N(y)$: drain is higher than the source $\Rightarrow$ less charge at drain end of channel
Gradual channel approximation

- We have played pretty fast and loose, using the average charge and average velocity, etc.
- A more accurate model of the physics includes the fact that the charge density under the gate and the velocity vary along the channel length.
- The current at each point along the length of the device must be independent of position in steady state (no buildup of charge).

\[ I_D = -W v_y(y) Q_N(y) \]

- Where \( I_D \) is the drain current, \( y \) is the distance in the direction from the source to the drain, \( v_y \) is the component of velocity in the source→drain direction, and \( Q_N(y) \) is the charge density of the electrons under the gate.

Gradual channel approximation -2

- For most FET’s the distances in \( y \), the Source→Drain direction, are significantly larger than the distances in the \( x \) direction, (perpendicular to the oxide).
- If this assumption is not true, its called a short channel device.
- This means that the fields in the \( x \) direction are much stronger than the fields in the \( y \) direction.
- This is in the text, section 4.3, with the main difference from the simple approximation being the back gate effect, due to the variation in the depletion width to the body (substrate).
**Effect of substrate voltage**

- What is the effect of different substrate voltages?
  - Depletion width $W$ changes
  - Need to account for different depletion region charge

\[
(V_{SB} = 0): \quad Q_{B0} = -\sqrt{2qN_Ae_S - 2\phi_p}
\]

\[
(V_{SB} \neq 0): \quad Q_B = -\sqrt{2qN_Ae_S - 2\phi_p + V_{SB}}
\]

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**Threshold voltage: general**

- General form (with substrate bias):

\[
V_T = V_{FB} - 2\phi_p - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}
\]

- Substituting the capacitance as a function of voltage:

\[
V_T = V_{T0} + \gamma \left(\sqrt{-2\phi_p + V_{SB}} - \sqrt{2\phi_p}\right)
\]

Where:

\[
\gamma = \frac{\sqrt{2qN_Ae_S}}{C_{ox}} \quad \text{+ for NMOS}
\]

\[
\gamma = \frac{2qN_Ae_S}{C_{ox}} \quad \text{- for PMOS}
\]
Threshold voltage, summary

- If $V_{SB} = 0$ (no substrate bias):
  \[
  V_{T0} = V_{FB} - 2\phi_p - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}
  \]

- If $V_{SB} \neq 0$ (non-zero substrate bias)
  \[
  V_T = V_{T0} + \gamma \left( \sqrt{-2\phi_p + V_{SB}} - \sqrt{2\phi_p} \right)
  \]

- Body effect (substrate-bias) coefficient:
  \[
  \gamma = \frac{\sqrt{2qN_A\varepsilon_S}}{C_{ox}} \quad (\text{NMOS})
  \]

- Threshold voltage increases as $V_{SB}$ increases. The threshold voltage will also vary along the gate. This is called the body effect, or back gate effect.

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Threshold Voltage (NMOS vs. PMOS)

<table>
<thead>
<tr>
<th></th>
<th>NMOS (p-substrate)</th>
<th>PMOS (n-substrate)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Fermi potential</td>
<td>$\phi_p &lt; 0$</td>
<td>$\phi_n &gt; 0$</td>
</tr>
<tr>
<td>Depletion charge density</td>
<td>$Q_B &lt; 0$</td>
<td>$Q_B &gt; 0$</td>
</tr>
<tr>
<td>Substrate bias coefficient</td>
<td>$\gamma &gt; 0$</td>
<td>$\gamma &lt; 0$</td>
</tr>
<tr>
<td>Substrate bias voltage</td>
<td>$V_{SB} &gt; 0$</td>
<td>$V_{SB} &lt; 0$</td>
</tr>
<tr>
<td>Threshold voltage (enhancement devices)</td>
<td>$V_{T0} &gt; 0$</td>
<td>$V_{T0} &lt; 0$</td>
</tr>
</tbody>
</table>
Body effect

- Voltage $V_{SB}$ changes the threshold voltage of transistor
  - For NMOS, Body normally connected to ground
  - For PMOS, body normally connected to $V_{cc}$
  - Raising source voltage increases $V_T$ of transistor

Threshold voltage adjustment

- Threshold voltage can be changed by doping the channel region with donor or acceptor ions
  - For NMOS:
    - The threshold voltage is increased by adding acceptor ions
    - The threshold voltage is decreased by adding donor ions
  - For PMOS:
    - The threshold voltage is increased by adding donor ions
    - The threshold voltage is decreased by adding acceptor ions
  - Approximate change in threshold voltage:
    - Density of implanted ions = $N_i$ [cm$^{-2}$]
    $$\Delta V_{T0} = \frac{qN_i}{C_{ox}}$$
Channel Length Modulation

- As $V_{DS}$ is increased, the pinch-off point moves closer to source, shortening the channel length.
- The drain current increases due to shorter channel:

$$L' = L - \Delta L$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^2 \left(1 + \lambda V_{DS}\right)$$

$\lambda = \text{channel length modulation coefficient}$

Review

Cutoff

$V_{GS} < V_{TN}$ implies $I_D = 0$

$V_{GS} < V_{TP}$

Linear

$V_{GS} \geq V_{TN}$, $V_{DS} < V_{GS} - V_{TN}$ implies $I_D = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2\right]$}

Saturation

$V_{GS} \geq V_{TN}$, $V_{DS} \geq V_{GS} - V_{TN}$ implies $I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \left(1 + \lambda V_{DS}\right)$

Note: if $V_{SB} \neq 0$, need to calculate $V_T$
NMOS

\[ V_{DS} = V_{GS} - V_T \]

Slope due to Channel length modulation

V\(_{\text{GS}}\) Steps

PMOS

\[ V_{DS} = V_{GS} - V_T \]

Slope due to Channel length modulation
• We now have reasonable mathematical models for NMOS and PMOS field effect transistors.
• We will now develop small signal models, allowing us to make equivalent circuits.
• The whole idea will be to make models that you can manipulate easily, and analyze and design circuits with FETs.
• We will also look at how SPICE models FETs for both small signal models and large signal models.

Small signal models: two terminals

The current into a device depends on the history of voltages which have been applied to it

$$I(t) = F\{V(\tau < t)\}$$

Let’s say this can be written as a function of the voltage, and its derivative with respect to time

$$I(t) = f\left(V(t), \frac{dV(t)}{dt}\right)$$

But that it is a nonlinear function.
Often we will be interested in running devices at a particular steady voltage or **operating point**, and then have the time varying signal be small compared to the DC voltage. We write this:

\[ V(t) = V_0 + v(t) \]

If we plug this back into our equation:

\[ I(t) = f(V(t), \frac{dV(t)}{dt}) = f(V_0 + v(t), \frac{dv(t)}{dt}) \]

Let’s assume that \( v(t) \) is very small, so we can do a Taylor expansion around 0.

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**linearization**

Taylor expansion about the first argument:

\[
f(x) \approx f(x_0) + x \left( \frac{df(x)}{dx} \right)_{x=x_0} + \cdots
\]

\[
I(t) \approx f\left(V_0, \frac{dv(t)}{dt}\right) + v(t) \left( \frac{\partial}{\partial V} f(V, \frac{dv(t)}{dt}) \right)_{V=V_0}
\]

Doing the same about the second argument:

\[
I(t) \approx f\left(V_0, \frac{dv(t)}{dt}\right) + v(t) \left( \frac{\partial}{\partial \xi} f(V_0, \xi) \right)_{\xi=0}
\]

We can then write:

\[
I(t) \approx I_0 + v(t) \left( \frac{1}{R} \right) \frac{dv(t)}{dt} + C \frac{dv(t)}{dt}
\]

Where

\[
I_0 = f(V_0,0) \quad \frac{1}{R} \left( \frac{\partial}{\partial V} f(V,0) \right)_{V=V_0} \quad C = \left( \frac{\partial}{\partial \xi} f(0,\xi) \right)_{\xi=0}
\]
From math to equivalent circuit

- We can then take:
  \[ I(t) = I_0 + i(t) \]

  Where \( i(t) \) is the small signal current. Then:
  \[ i(t) \approx v(t) \frac{1}{R} + \frac{dv(t)}{dt} C \]

- But this mathematical formula relating the small signal voltage to the small signal currents can be represented as a circuit again:

Which is why we picked \( R \) and \( C \), of course!

- Since a small change to a voltage or current into a device with other voltages or currents held constant generally results in a small, proportionate change, we can often model a device for small changes with linear equations.

- The linear equations can often be translated back into a circuit which would have the equivalent set of linear equations.

- Why would we do this? Because we can develop and use intuition about linear circuit elements, like resistors and capacitors, in series or parallel
Constructing by inspection

- Many times, rather than going through a process of deriving a mathematical formula and then translating it back into a circuit model, you can look at a device and create an equivalent circuit.
- Charge storage is modeled as a capacitor.
- Currents proportional to voltages are modeled by resistors.
- No model is perfect, build a simple model first, and then add to it as necessary.
- Remember: Parallel: current gets a choice
  Series: current must go through both.

VLSI resistor

- Let's construct a small signal model for a VLSI resistor:
Back to the FET

The current from the drain of our FET can be modeled for small signals:

\[ i_{DS}(t) = I_{DS} + i_{ds} \]

For a given operating point voltage for \( V_{gs} \) and \( V_{ds} \), we get:

\[ i_{ds} = \frac{\partial i_{DS}}{\partial V_{gr}} v_{gs} + \frac{\partial i_{DS}}{\partial V_{ds}} v_{ds} \]

Which we will then label:

\[ i_{ds} = g_m v_{gs} + \frac{1}{r_o} v_{ds} \]

Transconductance Conductance

Substrate potential

Lets look at the back gate effect in a small signal model

Effect: changes threshold voltage, which changes the drain current … substrate acts like a “backgate”

\[ g_{mb} = \frac{\Delta i_D}{\Delta V_{BS}} \bigg|_{Q} = \frac{\partial i_D}{\partial V_{BS}} \bigg|_{Q} \]

\[ Q = (V_{GS}, V_{DS}, V_{BS}) \quad \text{← are all held constant} \]
**Backgate Transconductance**

\[ V_T = V_{T0} + \gamma \left( \sqrt{V_{SB} - 2\phi_p} - \sqrt{-2\phi_p} \right) \]

Result:

\[ g_m = \left. \frac{\partial i_D}{\partial V_{gs}} \right|_Q = \left. \frac{\partial i_D}{\partial V_{gs}} \right|_Q \frac{\partial V_{gs}}{\partial V_{rs}} \bigg|_Q = \frac{\gamma g_m}{2\sqrt{V_{gs} - 2\phi_p}} \]

- Notice that we have terms in our equations which give the small signal current into one terminal in as a constant times the small signal voltage into another terminal. In order to translate that into an equivalent circuit, we will use variable current sources

\[ + \quad v_1 \quad \Diamond \quad i_2 = g v_1 \quad - \]

Where \( g \) is called the **transconductance**
Combining terms: Small-Signal Model

We now have three small signal contributions to the current into the drain terminal for our FET, from changes in $V_{gs}$, $V_{bs}$, and $V_{ds}$.

$$i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + \frac{1}{r_o} v_{ds}$$

Notice that the change in the small signal current into the drain from a small signal change in $V_{ds}$ can be modeled as a resistor.

Capacitances

- While adequate for some purposes, the model so far implies that the current into the gate is zero. This is a good approximation for low frequencies, for high frequencies we need to account for the current necessary to charge up the gate to supply the field across the oxide. There are also stray capacitances to the drain and source contacts.
MOSFET Capacitances in Saturation

The gate-drain capacitance is only the fringe capacitance when in saturation, because it is pinched off from the charge in the channel.

Gate-source capacitance: There is fringing charge between the edge of the gate and the source, but also to the channel

\[ C_{gs} = \frac{2}{3}WL + C_{ov} \]

Overlap capacitance along source edge of gate →

\[ C_{ov} = L_D W C_{ox} \]

(This is an underestimate, fringing fields will make the overlap capacitance larger)
**Gate-Drain Capacitance** \( C_{gd} \)

There is no contribution due to change in inversion charge in channel, just overlap capacitance between drain and source.

**Junction Capacitances**

The source, gate, and drain will also have capacitances between them and the well or substrate. Capacitances to the drain and source will be junction capacitances, and since \( V_{SB} \) and \( V_{DB} = V_{SB} + V_{DS} \) reverse biases are different, the capacitances will be different.
Seeking perfection…

- Remember that all of the capacitances, resistances and transimpedances will change as the operating point changes.
- There is no such thing as a perfect small signal model, use the simplest one that is sufficient.
- Sometimes a small signal model is used well outside of where it is accurate, because it is the main way we can deal intuitively with these devices!