Lecture 29: Diode connected devices, mirrors, cascode connections

Prof J. S. Smith

Context

Today we will be looking at more single transistor active circuits and example problems, and then starting multi-stage amplifiers

Lecture Outline

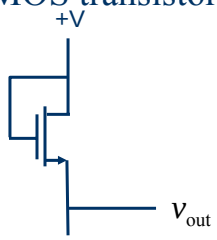
- Summary of single-transistor amplifiers
- Diode connected MOSFETs
- Current Mirrors
- Biasing Schemes

Single Stage Amplifiers

- Common-source is the only stage that provides both current and voltage gain
  - Miller effect limits high frequency response
- Common-drain can buffer a poor voltage source into a very good voltage source one
- Common-gate can buffer a poor current source into a very good current source, or replicate a current source into many current sources (current mirror)

NMOS pullup

- Rather than using a big (and expensive) resistor, let's look at a NMOS transistor as an active pullup device



Note that when the transistor is connected this way, it is not an amplifier, it is a two terminal device. When the gate is connected to the drain of this NMOS device, it will be in saturation, so we get the equation for the drain current:

$$I_D = \left(\frac{W}{2L}\right)\mu_n C_{ox}\left(V_{SG} - V_{Tn}\right)^2\left(1 + \lambda_n V_{SD}\right)$$

Small signal model

- So we have:

$$I_D = \left(\frac{W}{2L}\right)\mu_n C_{ox}\left(V_{SG} - V_{Tn}\right)^2\left(1 + \lambda_n V_{SD}\right)$$

$$= \left(\frac{W}{2L}\right)\mu_n C_{ox}\left(\Delta V - V_{Tn}\right)^2\left(1 + \lambda_n \Delta V\right) \approx \left(\frac{W}{2L}\right)\mu_n C_{ox}\left(\Delta V - V_{Tn}\right)^2$$

- The N channel MOSFET's transconductance is:

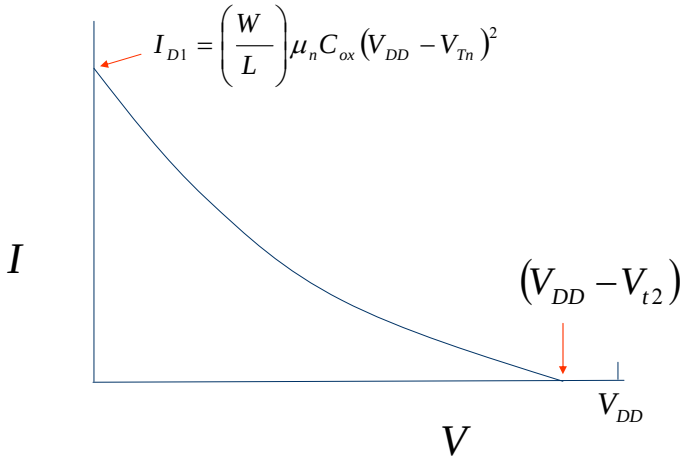
$$g_m = \frac{\partial}{\partial v_{SG}}\left(i_D\right)\Big|_Q = \left(\frac{W}{L}\right)\mu_n C_{ox}\left(V_{SG} - V_{Tn}\right) \cong \sqrt{2\left(\frac{W}{L}\right)\mu_n C_{ox}\left(I_D\right)}$$

- And so the small signal model for this device will be a resistor with a resistance:

$$r = \left(\frac{1}{g_m}\right)$$

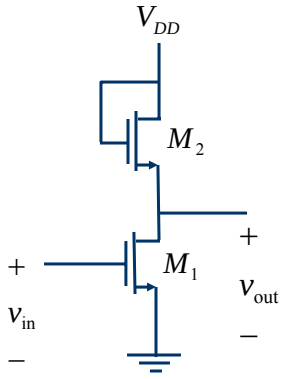
IV for NMOS pull-up

- The I-V characteristic of this pull-up device:



Active Load

- We can use this as the pullup device for an NMOS common source amplifier:



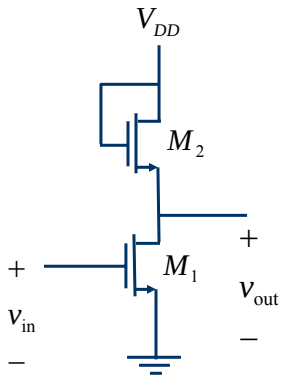
$$I_{D1} = \left(\frac{W_1}{2L_1}\right)\mu_n C_{ox}\left(V_{gs1} - V_{Tn1}\right)^2$$

$$I_{D2} = \left(\frac{W_2}{2L_2}\right)\mu_n C_{ox}\left(V_{gs2} - V_{Tn2}\right)^2$$

$$V_0 = V_{DD} - V_{gs2}$$

$$V_0 = V_{DD} - V_{t2} - \sqrt{\frac{2I_2}{\mu_n C_{ox}\left(W_2 / L_2\right)}}$$

Active Load



Since I_2=I_1 we have:

$$V_0 = V_{DD} - V_{t2} - \sqrt{\frac{2I_1}{\mu_n C_{ox}(W_2/L_2)}}$$

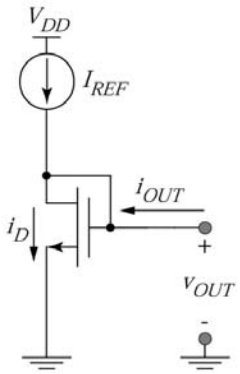
And since: $V_{gs1} = V_i$

$$V_0 = V_{DD} - V_{tn1} - \sqrt{\frac{(W_1/L_1)}{(W_2/L_2)}}(V_i - V_{t1})$$

Behavior

- If the output voltage goes higher than one threshold below VDD, transistor 2 goes into cutoff and the amplifier will clip.
- If the output goes too low, then transistor 1 will fall out of the saturation mode.
- Within these limitations, this stage gives a good linear amplification.

CMOS Diode Connected Transistor

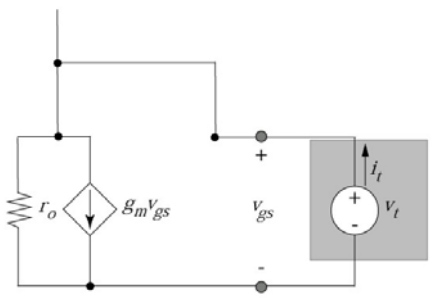


- Short gate/drain of a transistor and pass current through it
- Since VGS = VDS, the device is in saturation since VDS > VGS-VT
- Since FET is a square-law (or weaker) device, the I-V curve is very soft compared to PN junction diode

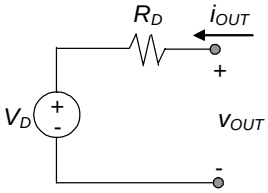
Diode Equivalent Circuit

$$R_D = \left(\left. \frac{di_{OUT}}{dv_{OUT}} \right|_{I_{OUT}=0} \right)^{-1} = \frac{v_t}{i_t}$$

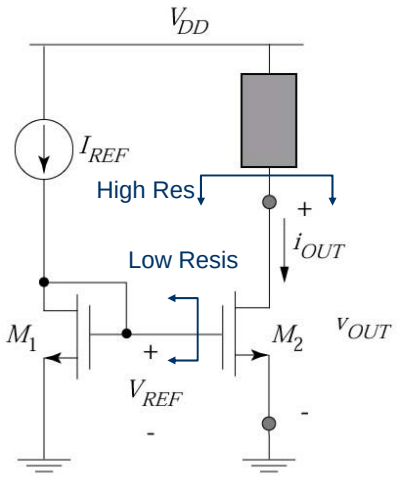
$$R_D \approx \frac{1}{g_m}$$



Equivalent Circuit:

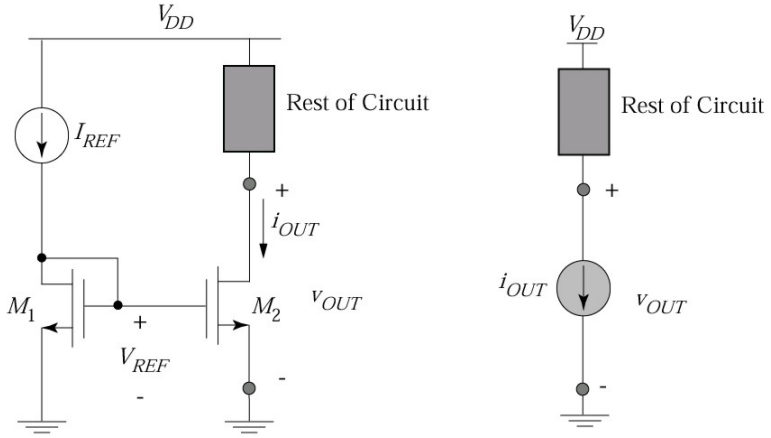


The Integrated "Current Mirror"



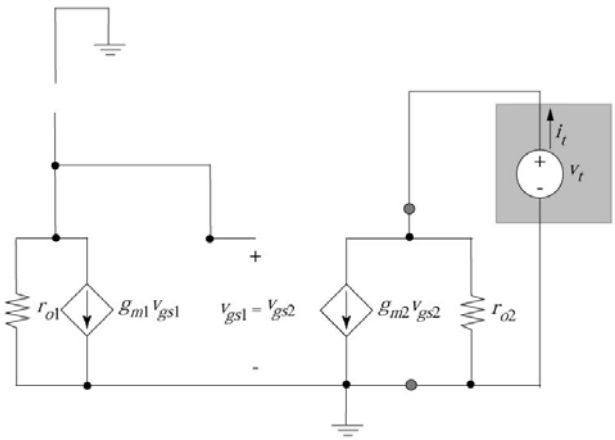
- M_1 and M_2 have the same V_{GS}
- If we neglect CLM (λ=0), then the drain currents are equal
- Since λ is small, the currents will nearly mirror one another even if V_{out} is not equal to V_{GS1}
- We say that the current I_{REF} is mirrored into i_{OUT}
- Notice that the mirror works for small and large signals!

Current Mirror as Current Source



- The output current of M_2 is only weakly dependent on v_{OUT} due to high output resistance of FET
- M2 acts like a current source to the rest of the circuit

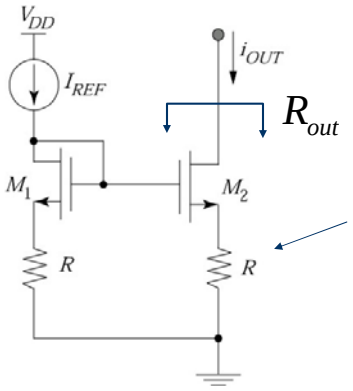
Small-Signal Resistance of *I*-Source



Improved Current Sources

Goal: increase r_{oc}

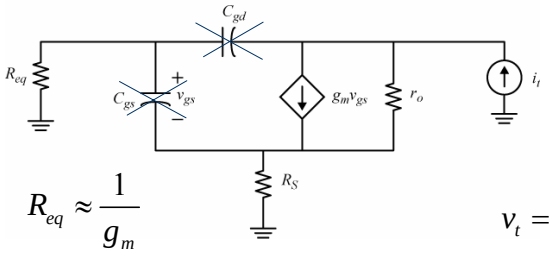
Approach: look at *amplifier* output resistance results … to see topologies that boost resistance



$R_{out} >> r_o$

Looks like the output impedance of a common-source amplifier with source degeneration

Effect of Source Degeneration



$$R_{eq} \approx \frac{1}{g_m}$$

$$v_t = (i_t - g_m v_{gs}) r_o + v_{R_S}$$

$$v_{gs} \approx -v_{R_S}$$

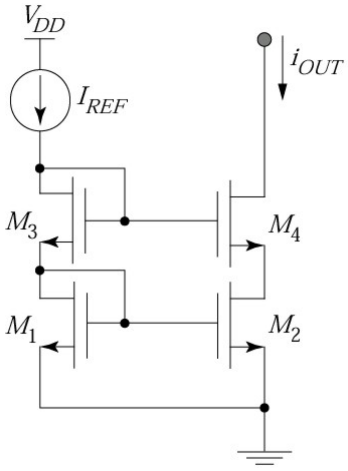
$$v_{R_S} = i_t R_S$$

$$v_t = (i_t + g_m R_S i_t) r_o + i_t R_S$$

$$R_o = \frac{v_t}{i_t} \approx (1 + g_m R_S) r_o$$

- Equivalent resistance loading gate is dominated by the diode resistance … assume this is a small impedance
- Output impedance is boosted by factor $(1 + g_m R_S)$

Cascode (or Stacked) Current Source



Insight: V_{GS2} = constant AND V_{DS2} = constant

Small-Signal Resistance r_{oc}:

$$R_o \approx (1 + g_m R_S) r_o$$

$$R_o \approx (1 + g_m r_o) r_o$$

$$R_o \approx g_m r_0^2 >> r_o$$

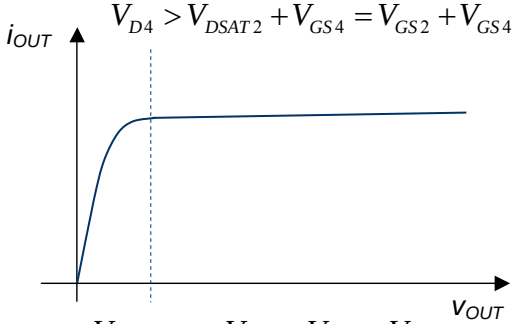
Drawback of Cascode *I*-Source

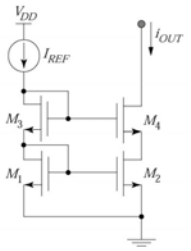
Minimum output voltage to keep both transistors in saturation:

$$V_{OUT,MIN} = V_{DS4,MIN} + V_{DS2,MIN}$$

$$V_{DS2,MIN} > V_{GS2} - V_{T0} = V_{DSAT2}$$

$$V_{D4} > V_{DSAT2} + V_{GS4} = V_{GS2} + V_{GS4} - V_{T0}$$



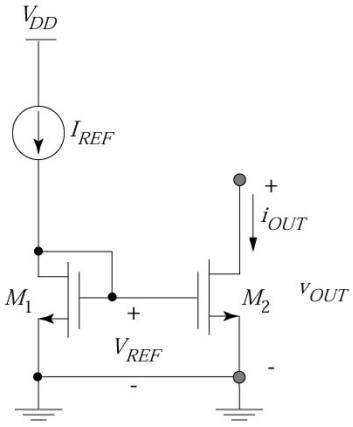


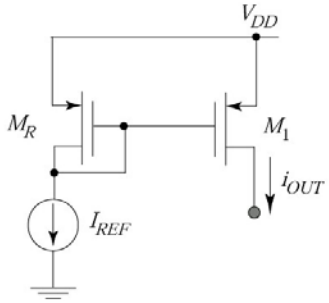
$$V_{OUT,MIN} = V_{GS2} + V_{GS4} - V_{T0}$$

Current Sinks and Sources

Sink: output current goes to ground

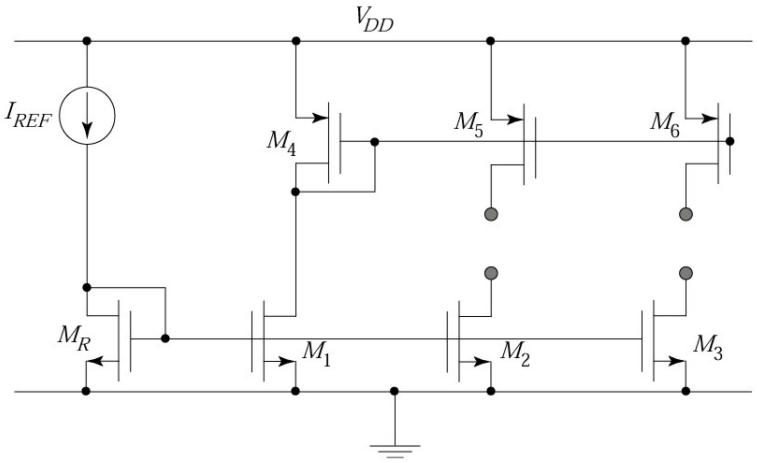
Source: output current comes from voltage supply





Current Mirrors

Idea: we only need one reference current to set up all the current sources and sinks needed for a multistage amplifier.



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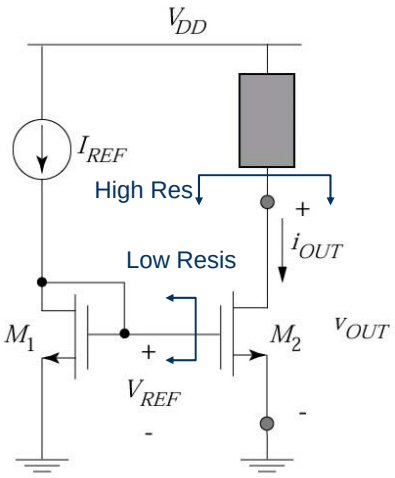

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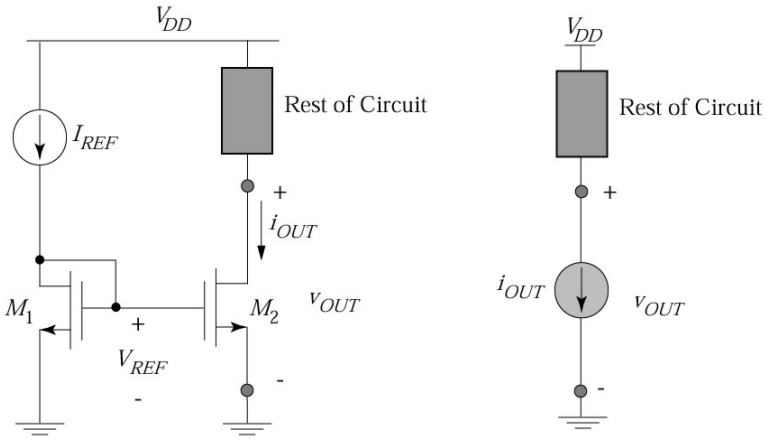

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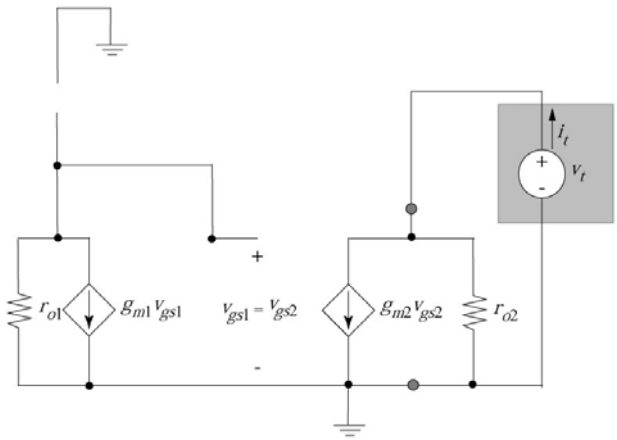

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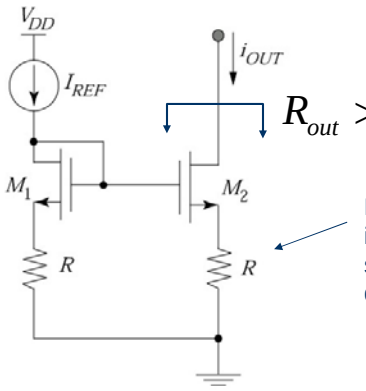

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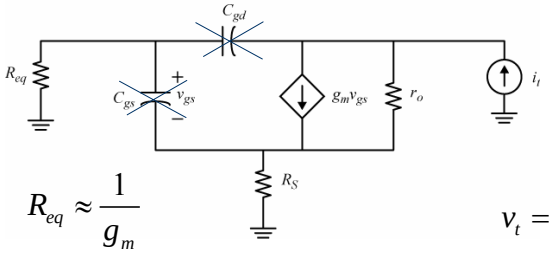

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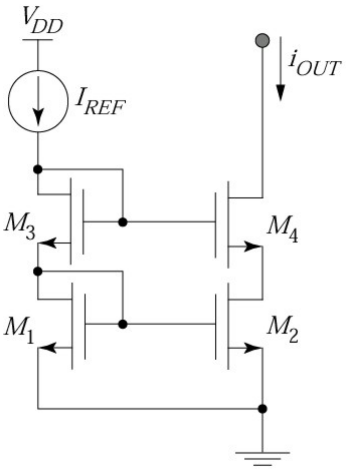

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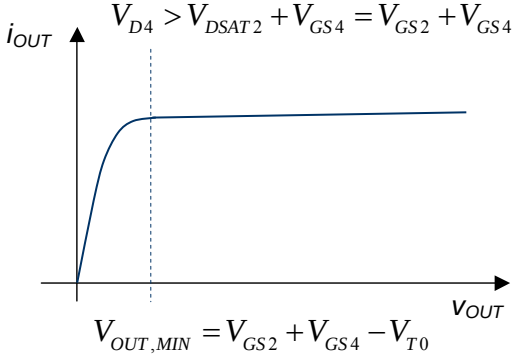

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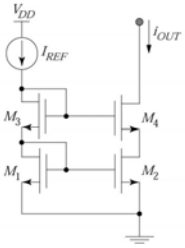

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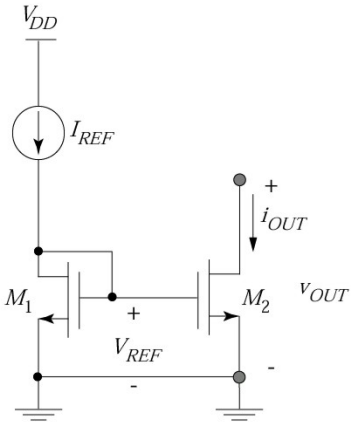

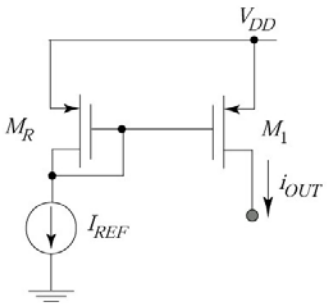

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