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**College of Engineering**
**Department of Electrical Engineering and Computer Sciences**

**Discussion Notes #3**

**EE 105** **Spring 2007**
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# 1 The MOS Capacitor

Last week, the lectures covered the operation of the MOS capacitor. Let's briefly review the material covered, in particular the regions of operation (i.e. accumulation, depletion, and inversion) and how to obtain a qualitative understanding of how the capacitance arrives in these regions of operation. I will assume an n+ gate an p-type substrate for this discussion.

## 1.1 Accumulation

Recall that accumulation occurs when we set $V_{GB} < V_{FB}$, pulling the gate to a potential below the substrate. From the graph of potential across the MOS structure (see Figure 1), we know that $\frac{dV}{dx}$ is positive, meaning $E(x)$, the electric field, is negative, or pointing in the negative $x$ direction. This causes holes to accumulate at the top of the substrate and electrons to accumulate at the bottom of the n+ gate.

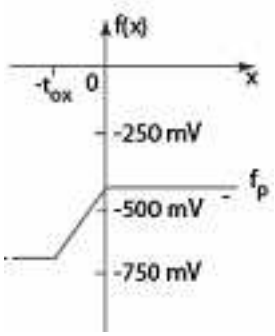


Figure 1: Potential across a MOS capacitor in accumulation.

This is exactly the behavior we imagine from a parallel plate capacitor. If we incrementally change $V_{GB}$ while the device is in accumulation, we're incrementally changing the slope of $V$, meaning we're incrementally changing $E(x)$, which is a constant value for a given $V_{FB}$. For a parallel plate capacitor, we have $C = \frac{\epsilon}{d}$, where $\epsilon$ is the permittivity of the dielectric material and $d$ is the distance between the separated charges. In this case, we have $\epsilon = \epsilon_{ox}$ and $d = t_{ox}$, so the capacitance in accumulation is $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$.

## 1.2 Depletion

Depletion occurs when $V_{FB} < V_{GB} < V_{Tn}$. Figure 2 shows the potential across the MOS capacitor when operating in the depletion mode.

We can see that for $-t_{ox} < x < 0$, the potential is still linear, as it was in accumulation. Hence, our physical interpretation would be that we still have the presence of $C_{ox}$ in the capacitance of the entire structure. However, we also have a depletion region now, meaning we have a depletion capacitance (Howe and Sodini call this $C_b$, presumably for bulk capacitance, so I will stick with that notation).

We know that the depletion region will have a certain width $X_d$, which depends on the applied $V_{GB}$. Although $X_d(V_{GB})$ is a rather complicated function, we know that for a given depletion width, the capacitance

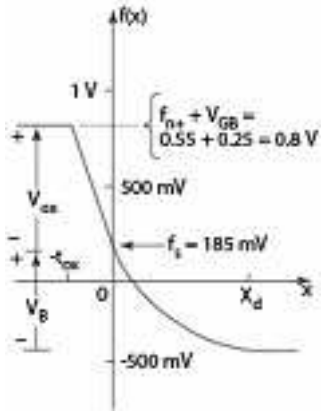


Figure 2: Potential across a MOS capacitor in depletion.

can be written as $C_b = \frac{\epsilon_s}{X_d}$. Since $C_b$ is in series with $C_{ox}$ ($C_{ox}$ represents the capacitance from $x = -t_{ox}$ to $x = 0$, while $C_b$ represents the capacitance from $x = 0$ to $x = X_d$), we can write $C = \frac{C_{ox}C_b}{C_{ox}+C_b}$.

Since $C_{ox}$ is a constant, we have the capacitance varying as a function of $C_b$. Consider qualitatively as $V_{GB}$ increases, the depletion width, $X_d$, increases, meaning that the capacitance $C_b \propto \frac{1}{X_d}$ decreases. Recall that for series capacitors, as one capacitance gets larger than the other, the equivalent capacitance approaches that of the smaller capacitor (think of the limiting case where the capacitance goes to zero). Hence, we would expect that the capacitance decreases as $V_{GB}$ increases while in the depletion mode of operation, and our intuition here corresponds with the actual device behavior.

## 1.3 Inversion

Inversion occurs when $V_{FB} > V_{Tn}$, where we define $V_{Tn}$ to be the threshold voltage of the device. We define $V_{Tn}$ to be the voltage where $\phi_s = -\phi_p$ (the exact reasons for this are related to energy bands and band bending, which is a topic for EE130). The simplified version of what is happening is that the silicon near the surface of the device (i.e. around $x = 0$) becomes inverted, meaning it actually starts acting like n-type silicon, despite being doped p-type. What this means is that electrons form at the surface, creating an inversion layer of charge.

Since this charge grows exponentially with the surface potential $\phi_s$ once $V_{FB}$ exceeds $V_{Tn}$ (see Eq. 3.135 in Howe and Sodini), we can make the approximation that $\phi_s$ remains approximately constant once the device hits inversion. This means that the depletion region stops growing and stays at $X_{d,max}$ while the inversion charge is free to grow very large as $V_{FB}$ is increased.

Having this foundation, we can once again use our physical intuition to determine the capacitance of the device. We know that if we change the voltage by a small amount $dV$, the depletion region won't grow at all, meaning there is no depletion capacitance in inversion. The positive charge in the n+ gate and the inversion charge at the surface of the substrate will change, though. Thus, we have $C = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$.

## 1.4 Frequency dependence (Optional)

There is a minor point to be made about the behavior of the device in inversion under high frequency and low frequency conditions. The electrons in the inversion layer must be generated somehow, as there aren't sufficient free electrons in a p-type substrate to form an inversion layer without some excitation. For a MOS capacitor as we have shown in our diagrams, the electrons are generated slowly by thermal excitation. For a high frequency signal, though, there is not sufficient time for this generation to occur, so we end up with $C_b$ (from our discussion of depletion) dominating the capacitance.

For MOS transistors, this isn't a problem, because we have n+ source and drain diffusions that have an ample supply of electrons to fill the inversion layer (called a channel once we talk about transistors). What this means is that under high frequency operation, instead of the capacitance jumping back up to $C_{ox}$ when

the device goes into inversion, it remains at the minimum value it reaches in depletion. Under low frequency operation, or when we have a source and drain, the capacitance does jump back up to $C_{ox}$.

## 1.5 Example Problem

Let's do an example problem. Assume we have a MOS capacitor with n+ polysilicon as the gate and p-type silicon as the substrate. Take $N_a = 10^{17}\text{cm}^{-3}$ for the substrate and $t_{ox} = 20\text{nm}$.

For this structure, we can compute $\phi_{n+}$ and $\phi_p$, the potentials of the gate and the substrate, respectively. From this, we can compute $V_{FB} = -(\phi_{n+} - \phi_p)$.

$$\begin{aligned}
\phi_{n+} &= 550\text{mV} \\
\phi_p &= -60\text{mV} \log \frac{N_a}{n_i} = -420\text{mV} \\
V_{FB} &= -(\phi_{n+} - \phi_p) = -(550 - (-420)) = -970\text{mV}
\end{aligned}$$

Now that we have the flatband voltage, we can also compute the threshold voltage.

$$\begin{aligned}
C_{ox} &= \frac{\epsilon_{ox}}{t_{ox}} = 172.6\text{nF/cm}^2 \\
V_{Tn} &= V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2q\epsilon_s N_a(-2\phi_p)} \\
&= 837\text{mV}
\end{aligned}$$

We have almost enough to plot the CV curve of this device. We know that for $V_{GB} < V_{FB}$ and $V_{GB} > V_{Tn}$, the capacitance is $C_{ox}$. We also have a qualitative feel for the capacitance for $V_{FB} < V_{GB} < V_{Tn}$ in that it will drop to a minimum until inversion occurs and the capacitance jumps back up to $C_{ox}$. Thus, we just need to find that minimum, then we can plot the CV curve.

We know that this capacitance value depends on $X_{d,max}$, so let's find that first.

$$\begin{aligned}
V_{B,max} &= \phi_s - \phi_p = -2\phi_p = 840\text{mV} \\
X_{d,max} &= \sqrt{\frac{2\epsilon_s V_{B,max}}{qN_a}} = 104.2\text{nm}
\end{aligned}$$

Now we can find the minimum value of $C_b$ by $C_{b,min} = \frac{\epsilon_s}{X_{d,max}} = 99.37\text{nF/cm}^2$. In depletion, the capacitance is $\frac{C_{ox}C_b}{C_{ox}+C_b}$, so using $C_{b,min}$ we have $C = 63.06\text{nF/cm}^2$. Figure 3 shows the qualitative plot of the CV characteristics of this MOS capacitor.

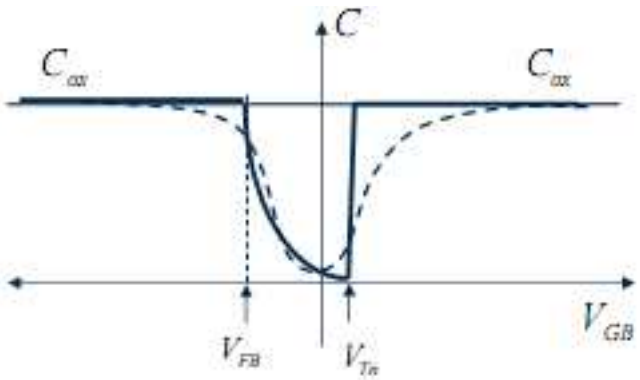


Figure 3: CV characteristics of a n+ gate, p-type substrate MOS capacitor.