UNIVERSITY OF CALIFORNIA AT BERKELEY
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Discussion Notes #4

EE 105 **Spring 2007**
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I) MOS Transistor

I_D Curve Derivation

The I_D equation of a MOS transistor is an important equation for the understanding of circuits. In the following discussion, we will derive the equations for the transistor in all modes of operation (cutoff, triode, and saturation). A similar explanation can be found in section 6.2.2 of Rasavi.

From your physics classes, recall the relation between capacitance, charge, and voltage:

$$C = \frac{Q}{V} \qquad (1)$$

Given the thickness of the oxide, we can calculate the gate capacitance per unit area C_{ox}

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad (2)$$

To find the capacitance per unit length of the oxide, we must multiply equation (2) by the width of the transistor. As shown in figure 1, the width is defined by W.

$$C = W \cdot C_{ox} \qquad (3)$$

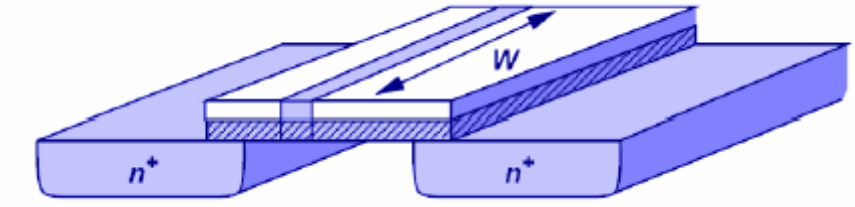

Figure 1: 3-D View of a basic transistor layout.

Using equation (1) we can now find the total charge on the substrate – oxide interface. Although the voltage applied across the oxide is V_{GS} (as seen in figure 2), charge does not start collecting at the substrate until inversion occurs, just as in a MOS capacitor. Inversion

only occurs when $V_{GS} > V_{TH}$, therefore, the charge at the silicon – oxide interface can be described as:

$$Q = W \cdot C_{ox} \cdot (V_{GS} - V_{TH}) \tag{4}$$

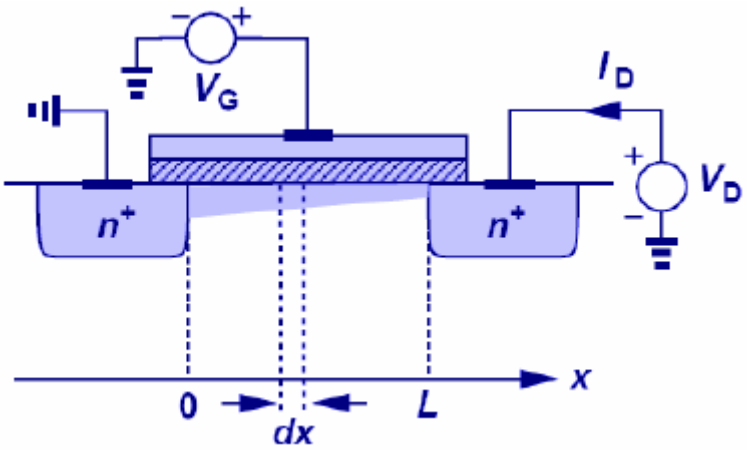

Figure 2: Transistor under applied voltages V_{GS}, and V_{DS}.

During normal operation, a transistor will have an applied voltage difference between the source and drain, V_{DS}. As a result, the voltage between the gate and the oxide decreases towards the positive x direction in figure 2. The reason is because the drain is at a higher potential than the source, and thus the potential difference between the gate and the oxide decreases from the source to the drain. As a result, the charge equation is now:

$$Q = W \cdot C_{ox} \cdot (V_{GS} - V(x) - V_{TH}) \tag{5}$$

Now that we have an accurate description of the charge at the silicon-oxide interface as a function of x, we can begin to derive the current equation. Recall:

$$I = Q \cdot v \tag{6}$$

$$v = -\mu_n \cdot E$$
$$v = \mu_n \cdot \frac{dV}{dx} \tag{7}$$

Equation 6 describes the definition of current, I. Equation 7 describes electron velocity as a function of an electric field. Plugging equation (5) and (7) into equation (6) we obtain

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx} \tag{8}$$

To solve the differential equation, we bring the dx to the left hand side, and integrate both sides

$$\int_{x=0}^{x=L} I_D dx = \int_{V(x)=0}^{V(x)=V_{DS}} WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n dV \tag{9}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS} - V_{TH})V_{DS} - V^2{}_{DS}] \tag{10}$$

Solving equation (9) gives us equation (10). If you plot equation (10), you will get a downward pointing parabola, as in Figure 3. The maximum current achievable, is

$$I_{D,\max} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{11}$$

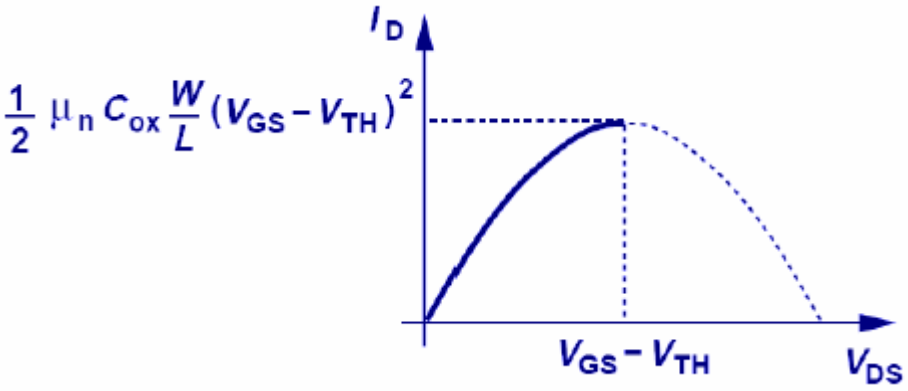

Figure 3: Plot of Equation (10).

II) REGIONS OF OPERATION

Triode

For NMOS: When $V_{DS} \leq V_{GS} - V_{TH}$, and $V_{GS} \geq V_{TH}$, the transistor is said to be in triode. In figure 3, it is the left hand side of the parabola. The common equation for the current in triode comes from equation (10). (For PMOS: $V_{SD} \leq V_{SG} + V_{TH}$, and $V_{SG} \geq -V_{TH}$)

$$I_{D,triode} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH} - \frac{V_{DS}}{2})V_{DS} \tag{12}$$

Saturation

For NMOS: When $V_{DS} \geq V_{GS} - V_{TH}$ and $V_{GS} \geq V_{TH}$, the transistor is said to be in saturation. The current stays constant at $I_{D,max}$ defined in equation (11) during saturation. The reason is due to pinch off. See figure 6.12 in Rasavi for more explanation. Equation (11) is the common equation for the current in saturation, it is reproduced below for ease. (For PMOS: $V_{SD} \geq V_{SG} + V_{TH}$ and $V_{SG} \geq -V_{TH}$)

$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

Cut-Off
For NMOS: When $V_{GS} \leq V_{TH}$, the substrate is not inverted, and thus no current can flow, $I_D = 0$. (For PMOS: $V_{SG} \leq -V_{TH}$)

III) Example Problems

1) **Region of Operation NMOS**: Determine the regions of operation for the following different NMOS transistor configurations. Assume $V_{TH} = 0.4V$

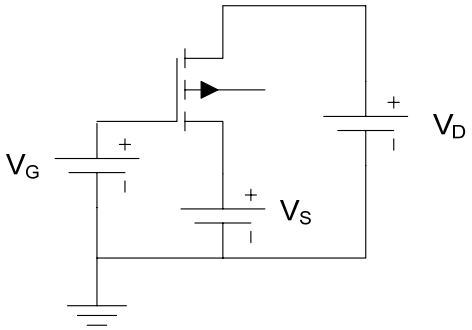

Figure 4: NMOS

a) $V_G = 1V$, $V_S = 0V$, $V_D = 0.5V$. Region: Triode, $V_{DS} = 0.5V < 0.6V = (V_{GS} - V_{TH})$
b) $V_G = 0.7V$, $V_S = -0.4V$, $V_D = 0V$. Region: Triode, $V_{DS} = 0.4V < 0.7V = (V_{GS} - V_{TH})$
c) $V_G = 0.3V$, $V_S = -1V$, $V_D = 0.2V$. Region: Saturation, $V_{DS} = 1.2V > 0.9V = (V_{GS} - V_{TH})$

2) **Region of Operation PMOS:** Assume the transistor is now a PMOS transistor, find the regions of operations. Assume $V_{TH} = -0.4V$

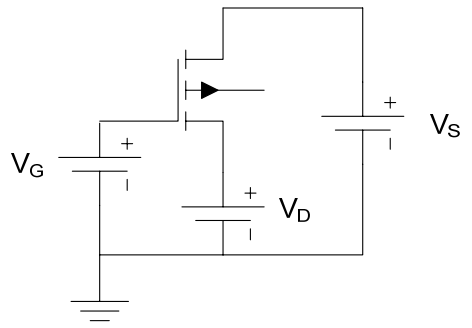

Figure 5: PMOS

d) $V_G = 0V$, $V_S = 1V$, $V_D = 0.5V$. Region: Triode, $V_{SD} = 0.5V < 0.6V = (V_{SG} + V_{TH})$
e) $V_G = 0.2V$, $V_S = 0.5V$, $V_D = -0.3V$. Region: Cutoff, $V_{SG} = 0.3V < 0.4V = -V_{TH}$
f) $V_G = 0V$, $V_S = 0.6V$, $V_D = 0.2V$. Region: Saturation, $V_{SD} = 0.4V > 0.2V = (V_{SG} + V_{TH})$

3) **90nm Technology.** Consider the circuit in figure 6. What is the smallest we can size the NMOS transistor with 90nm technology such that the out voltage $V_{OUT} = 2V$? Assume $V_{TH} = 0.4V$, and $\mu_n C_{ox} = 2.22*10^{-4}$ F/V*s.

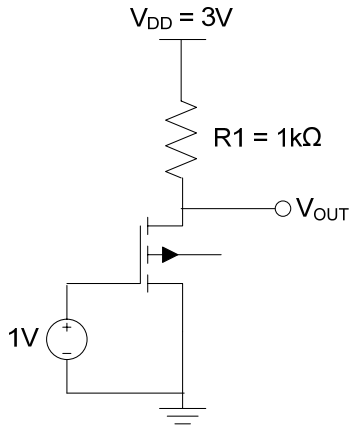

Figure 6: NMOS Biasing circuit.

$$I_D = \frac{V_{DD} - V_{OUT}}{R_1} = \frac{3V - 2V}{1000\Omega} = 1mA$$

$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$1mA = \frac{1}{2}2.22\times10^{-4}\frac{F}{cm^2}\frac{W}{L}(1V - 0.4V)^2$$

$$\frac{W}{L} = 25$$

$$L_{\min} = 90nm$$

$$W_{\min} = 2.25\mu m$$