UNIVERSITY OF CALIFORNIA AT BERKELEY
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Discussion Notes #6

EE 105 **Spring 2007**
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Cascodes & Current Mirrors

Cascodes are useful for providing a high output impedance current source. Current mirrors are generally used to copy a reference current (which consists of complex circuits that take up a large area of an IC) to other elements in the circuit.

Let's look at an example circuit that uses cascodes and current mirrors. Here, we want to make a MOS transconductance amplifier with the following specifications:

G_m = 1 mS
R_{out} > 10 MΩ
R_{in} → ∞
The output is a capacitive load (i.e. other MOSFETs)

We also have the following specifications for the circuit:

V_{DD} = 5 V
The circuit is made with a 2.0 μm CMOS process (means that L = 2 μm)
All transistors are biased at 100 μA
λ_n = 0.05 V^{-1} and λ_p = 0.02 V^{-1}
V_{Tn} = 1 V and V_{Tp} = -1 V
$\mu_n C_{ox}$ = 50 μA/V^2 and $\mu_p C_{ox}$ = 25 μA/V^2

We want to design a circuit architecture to meet this specification, as well as solve for the device dimensions and bias voltages.

Based on these specifications, the output resistance of a single transistor is given by:

$$r_0 = \frac{1}{\lambda I_D} = (1\text{ V}) / [(0.05\text{ V}^{-1})(100\ \mu\text{A})]$$
$$= 200\ \text{k}\Omega$$

Thus, the output resistance of a single transistor is too small to satisfy our requirements. To increase the output resistance, let's use a cascode amplifier (Fig. 1).

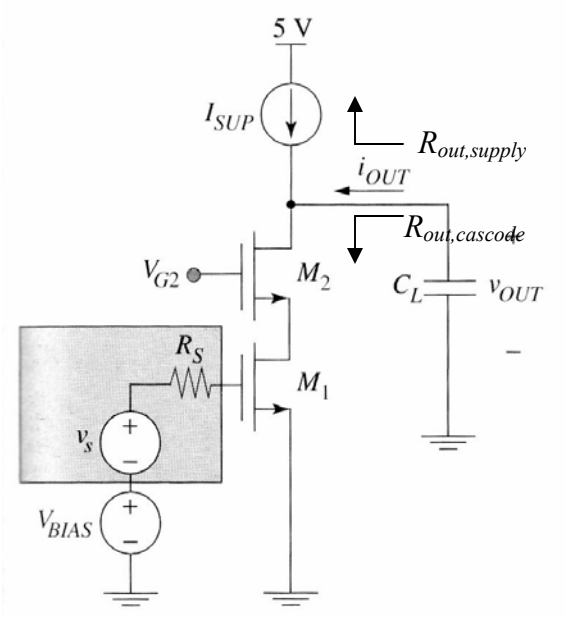

Fig. 1: Cascode amplifier

The transconductance of the cascode amplifier is given by:

$$G_m = g_{m1} = \sqrt{2\left(\frac{W}{L}\right)_1 \mu_n C_{ox} I_D} \qquad (1)$$

Plug in the given and known values into Eq. 1 (G_M = 1 mS, L = 2 μm, $\mu_n C_{ox}$ = 50 μA/V^2, and I_D = 100 μA) and you result in W_1 = 200 μm.

The output resistance of the cascode is given by:

$$R_{out,cascode} \approx g_{m2} r_{01} r_{02}$$

In addition, we want the R_{out} of the entire amplifier circuit to be 10 MΩ or greater. The total R_{out} is given by:

$$R_{out,total} = R_{out,supply} \,||\, R_{out,\ cascode}$$

where $R_{out,supply}$ is the output resistance of the current source of the cascode amplifier. Let's assume that $R_{out,supply} = R_{out,\ cascode}$, so the output resistance of each must be 20 MΩ or more to meet the design specification. Knowing that $R_{out,\ cascode}$ = 20 MΩ, we can solve for g_{m2} and W_2:

$$R_{out,cascode} = 20\ \text{M}\Omega \approx g_{m2} r_{02} r_{01}$$

$$g_{m2} = 20\ \text{M}\Omega / [(200\ \text{k}\Omega)\ (200\ \text{k}\Omega)] = 0.5\ \text{mS}$$

$$\left(\frac{W}{L}\right)_2 = \frac{g_{m2}}{2\mu_n C_{ox} I_D} \rightarrow W_2 = 50\ \mu\text{m}$$

We still need to have a large $R_{out,supply}$. We can achieve this with a PMOS cascode (Fig. 2). What gate voltages are needed for this circuit? We are constrained by the PMOS saturation condition: $V_{SD} > V_{SG} + V_{Tp}$. Let's pick V_{SG} = 1.5 V. The choice of V_{SG} is semi-arbitrary, but a smaller V_{SG} would mean that W/L would have to increase in order to keep I_D at 100 μA. Our choice of V_{SG} = 1.5 V means that V_{G4} = 5 V-1.5 V = 3.5 V. Let's also assume that $V_{SG} = V_{SD}$ (the reason will become clear later as we create the circuit to provide the gate biases), so that V_{S3} = 3.5 V, V_{G3} = 2.0 V, and V_{D3} = 2.0V.

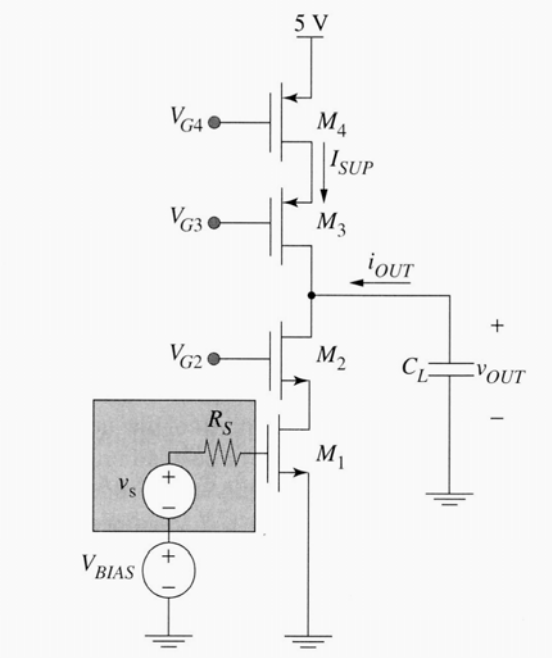

Fig. 2: NMOS cascode with PMOS cascode as a current load

Now, let's solve for widths of M3 and M4:

$$I_{D4} = I_{D3} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_4 \left(V_{SG} + V_{Tp}\right)^2$$

$$W_4 = W_3 = 64\ \mu\text{m}$$

We have to check to make sure the output resistance of the PMOS cascode is greater than 20 MΩ:

$$r_{03} = r_{04} = \frac{1}{\lambda_p I_D} = 500\ \text{k}\Omega$$

$$g_{m3} = \sqrt{2\left(\frac{W}{L}\right)_3 \mu_p C_{ox} I_D} = 0.4\ \text{mS}$$

$$R_{out,supply} \approx g_{m3} r_{03} r_{04} = 100\ \text{M}\Omega$$

We still need to create the bias voltages for V_{G4}, V_{G3}, and V_{G2}. We can do this with diode-connected MOSFETs (Fig. 3).

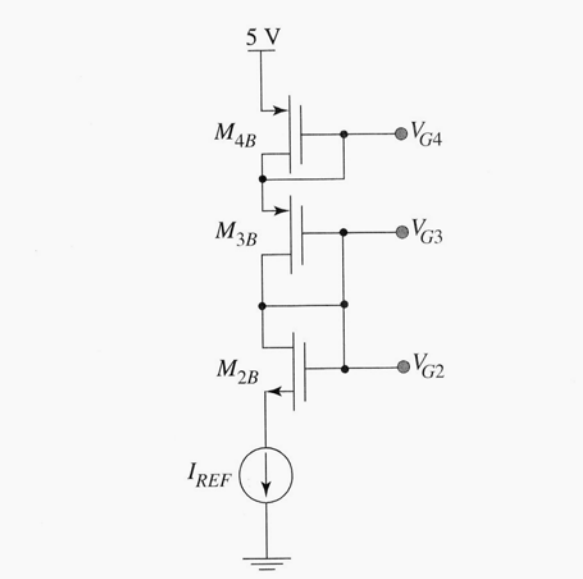

Fig. 3: Bias circuit for cascode amplifier

Let's make M_{4B} and M_{3B} have the same sizes as transistors M_4 and M_3. This matches the currents flowing through the transistors, and simplifies the design. Similarly, we want M_{2B} and M_2 to have the same V_{DS}, so we make these transistors the same size as well. Now we can solve for the value of V_{GS2}:

$$V_{GS2} = V_{GS2B} = V_{Tn} + \sqrt{\frac{2I_{REF}}{\left(\frac{W}{L}\right)_2 \mu_n C_{ox}}} = 1.4 \text{ V}$$

The completed circuit architecture is shown in Figure 4. We still need to solve for V_{BIAS} by using the saturation current equation:

$$V_{BIAS} = V_{Tn} + \sqrt{\frac{2I_{REF}}{\left(\frac{W}{L}\right)_1 \mu_n C_{ox}}} = 1.2 \text{ V}$$

We still have that $V_{DS1} > V_{BIAS} - V_{Tn}$, so M_1 is in saturation.

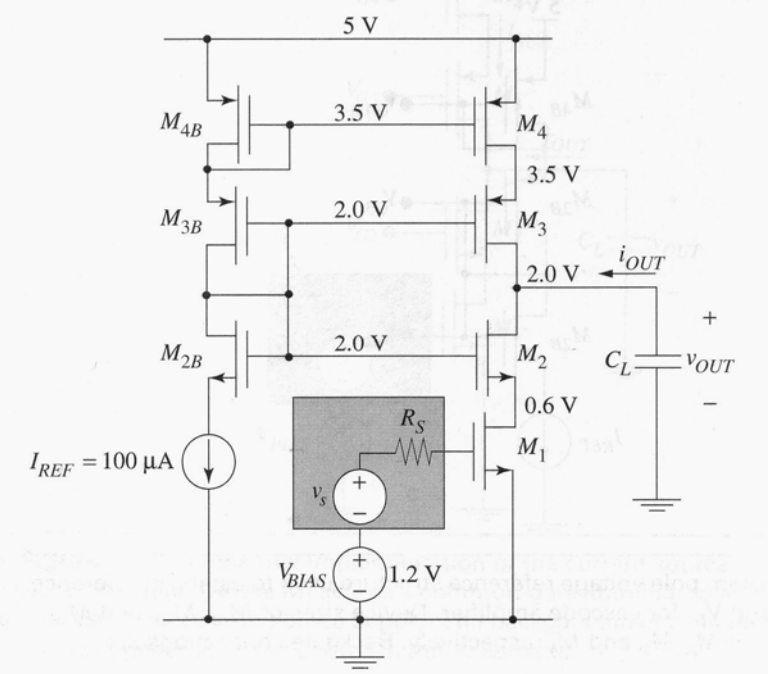

Fig. 4: Completed MOS transconductance amplifier. Note that the bias circuit acts as current mirrors for the cascode circuit.

What is the output voltage swing? In order to keep the PMOS devices in saturation, we must have $V_{SD} > V_{SG} + V_{Tp}$ → $V_{SD} > 0.5$ V. Thus, V_{D3} must be less than or equal to 3.0 V to keep M_3 in saturation. Similarly, for the NMOS devices, we must have $V_{DS} > V_{GS} + V_{Tn}$ in saturation. Since $V_{GS2} = 1.4$V, $V_{S2} = 0.6$V. We need V_{D2} to be greater than 1.0 V to remain in saturation. Thus, the output voltage can swing from 1.0 V to 3.0 V.