# Experiment 8
# Frequency Response

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## 1.0 Objective

This lab will introduce the student to frequency response of circuits. The student will be introduced to dominant pole analysis and the Miller effect. The student will look at gain and phase relationship of a common source amplifier with a 2-pole response. The key concepts introduced in this experiment are:

- Bode plot of frequency response
- dominant pole analysis

## 2.0 Prelab

- H & S: Chapter 10.1 - 10.3

**Q1.** For the circuit in Fig. 3, derive an expression for $v_{out}$(t) for both a high to low transition and a low to high transition. Your EE 40 textbook may help.

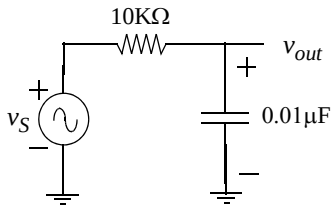


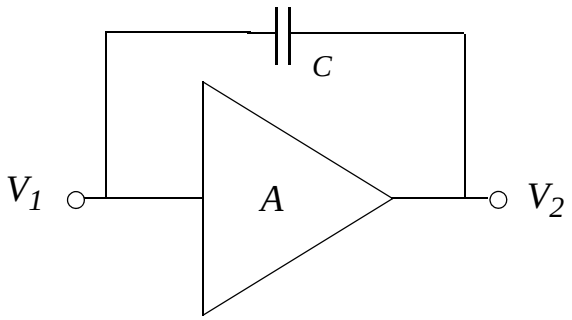

Figure P

**Q2.** For the circuit in Fig. P, derive the phasor expression $\frac{V_{out}(j\omega)}{V_s(j\omega)}$. See the notes on Bode plots in the Appendix on phasor analysis.

**Q3.** Find $V_{OUT}(\omega)$ : (sinusoid) at $\omega = 2\pi \times 1000$ . Amplitude and phase.

- The Miller Effect plays an important role in determining the poles of an amplifier. Shown below is a simple example.

**FIGURE 1.** Amplifying block with “Miller” capacitor




If there is a gain A across the capacitor C, the current across C can be written as

$$i = C\frac{\mathrm{d}}{\mathrm{d}t}(v_1 - v_2) = C\frac{\mathrm{d}}{\mathrm{d}t}(v_1 - Av_1)$$

This simplifies to

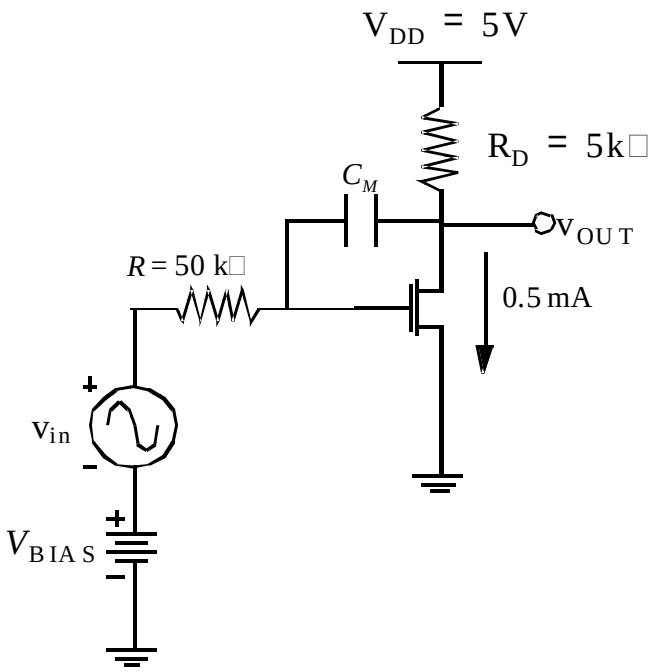
$$i = C(1 - A)\frac{\mathrm{d}}{\mathrm{d}t}(v_1)$$

So the equivalent capacitance looking into $v_1$ is the capacitance $C$ multiplied by (1 - $A$). If $A$ is sufficiently high, that capacitance will dominate and be the cause of the dominant pole.

**Q4.** For the common source amplifier below, determine the poles of the system ($g_m$ = 0.02mS, $\lambda = 0.02V^{-1}$). Use $C_\mu$= 50 fF and $C_{gs}$= 1.15 pF.

**Q5.** Derive the entire transfer function ($V_{out}$ / $V_{in}$) that includes $C_\mu$, $C_{gs}$ and general capacitances at the input (gate-source) and across the gain block (gate-drain). This general expression will be useful in determining the expected values for the measurements. The effect of a capacitive load connected to the output is not easily incorporated into the analytical transfer function. However, the location of this pole can be estimated by the product of the load capacitance and the small-signal resistance between the the output node and small-signal ground.

**FIGURE 2.** Common Emitter Amplifier to Demonstrate Miller Capacitance

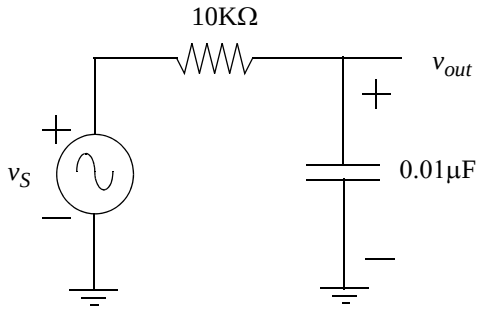


# 3.0 Procedure

## 3.1 Frequency and Time Domain Response

**1.** Construct the following lowpass filter circuit.

**FIGURE 3.** Lowpass Filter Circuit




**2.** Let $v_s$ be a sine wave with a frequency of 1kHz.

**3.** Place channel 1 of the oscilloscope at $v_s$ and channel 2 at $v_{out}$.

**4.** Display both waveforms on the oscilloscope. Sketch the waveforms and label all the relevant points.

**5.** How does $v_{out}(t)$ compare with the results from prelab?

**6.** With the gain-phase meter, connect channel A to the input and channel B to $v_{out}$.

**7.** Vary the frequency of a sine wave $v_s$ from 100 Hz to 100 kHz. Plot the ratio B/A as well as the phase. From the data you obtained. Sketch the Bode plot for the lowpass filter. (magnitude and phase) Label the -3dB point.

**8.** How does $\frac{v_{out}(j\omega)}{v_s(j\omega)}$ compare with the results from prelab?

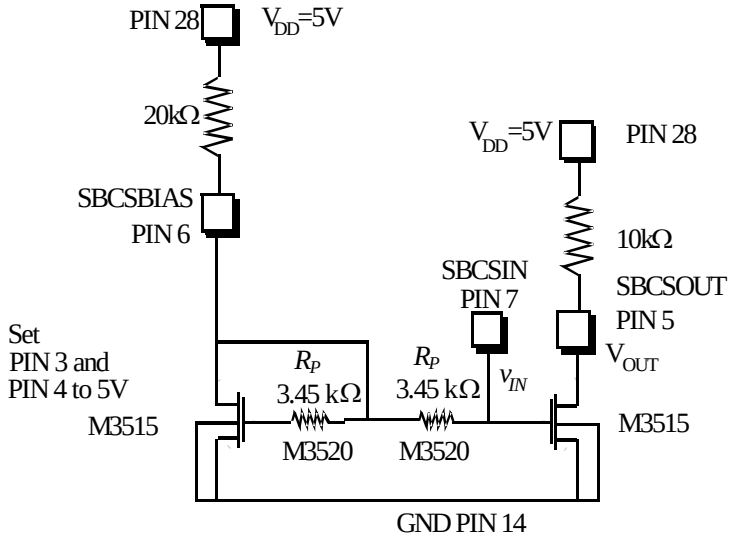
## Lab Tip

When using the gain-phase meter, make sure you use matched probes (1x or 10x) for channel A and channel B.

It is also advisable to observe the waveforms on the oscilloscope.

### 3.2 Frequency Response of the Common Source Amplifier

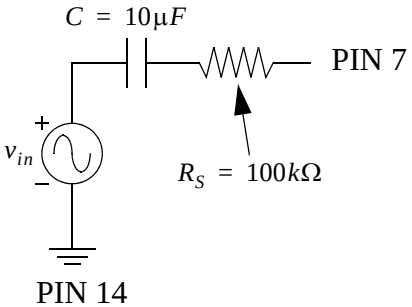
**FIGURE 4.** Common Source Amplifier with Resistor Load (SBCE_IN, Lab Chip 3)




Note: the $R_P$ = 3.45Ω resistors are on-chip.

1. Construct the self- biased Common Source found on Lab Chip 4, as shown in Fig. 4.
2. What is $I_{BIAS}$ and the DC voltage at $V_{OUT}$?
3. Insert the following signal into $v_{IN}$, as shown in Fig. 5. Let the amplitude of the small signal be 500 mV and the frequency be 100 Hz

**FIGURE 5.** Input Signal into Common Emitter Amplifier




4. Using the oscilloscope or the gain phase meter, find the gain $v_{out}/v_{in}$.
5. Now increase the frequency until the output decreases by a factor of 0.707 (-3dB). Note also the phase at this frequency. Is the phase consistent with the magnitude?

6. Make a Bode plot of the gain (both magnitude and phase) and observe the slope.

## Lab Tip

At higher frequencies, the input signal will begin to attenuate to the point that the gain-phase meter will not be able to detect it. You can compensate by increasing the amplitude of the signal generator. The oscilloscope is helpful in determining if the amplitude of the input waveform needs to be increased.

On the gain-phase meter, changing the phase reference dial from A to -A will either give you a starting reference of 0 or -180 degrees. Pick one and be consistent.

It is helpful to have the oscilloscope monitoring the waveforms so you can see it at all time.

Take data at 1, 2 and 5 of each decade.

Do a frequency sweep from about 100Hz to 5MHz.

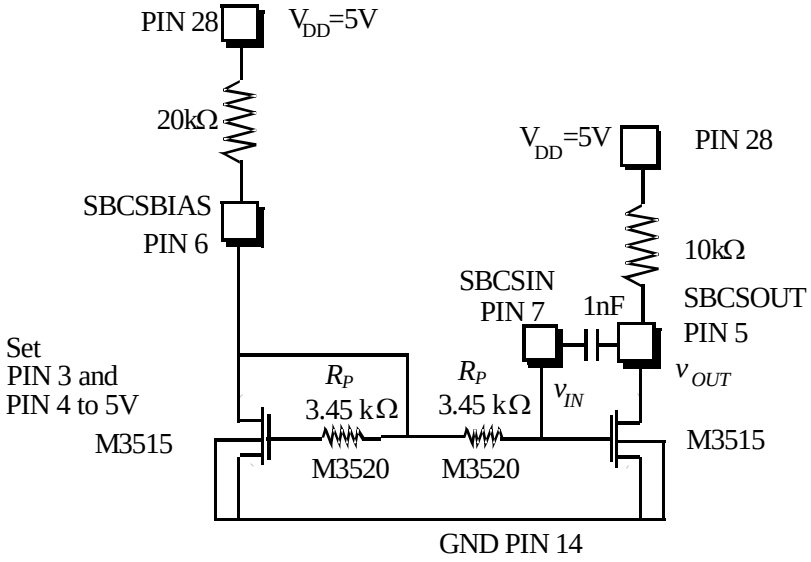
If you are using the gain-phase meter, make sure that the settings are the correct ones and keep in mind that in order to read the right phase, the amplitude may need to be increased at high frequencies.

7. Continue to increase the frequency and try to find the second pole. How will you know when you have found it?
8. Draw the small signal model for this amplifier. Where are the poles of this system? Where do the capacitances come from? Do your results agree?

### 3.2.1 Miller Effect

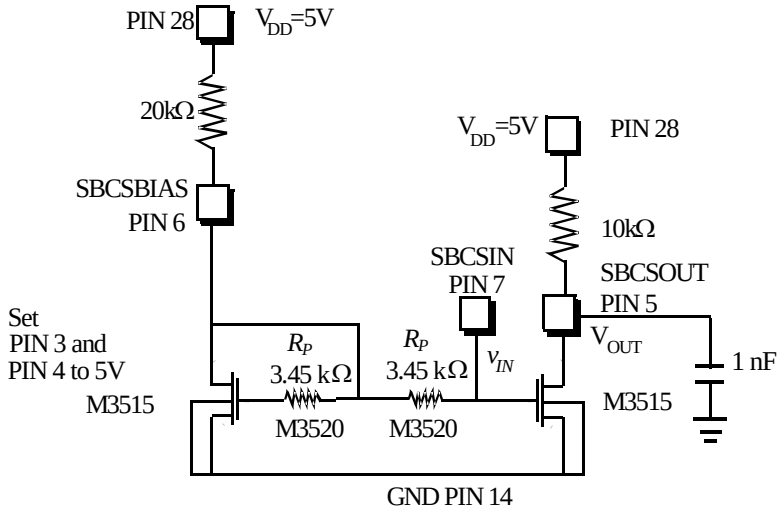
1. Construct the self biased common emitter amplifier found on Lab Chip 4 as shown in Fig. 6.
2. Repeat the above procedures to find the frequency response of this amplifier.

**FIGURE 6.** Self Biased Common Source Amplifier (Lab Chip 4) with Miller Capacitor




### 3.2.2 Common Source with Capacitor at the Output

**FIGURE 7.** Common Source with Capacitor at the Output (Lab Chip 4)



**1.** Repeat the procedures of the previous experiment with the configuration as shown in Fig. 7.

**2.** How do the results compare with the expected value of the new pole?

### 3.3 Common-Drain Frequency Response

1. By referring to Exp. 8, Fig. 4 of this lab manual, construct the common-drain amplifier.
2. Measure the DC voltage $V_{OUT}$ and the DC drain current $I_D$.
3. Apply a sinusoidal input signal with an amplitude of 500 mV and a frequency of 100 Hz at the input.
4. Determine the -3 dB frequency of this amplifier's transfer function $V_{out}/V_{in}$. Note that this stage is "wideband" and can have a high - 3 dB frequency, if the parasitic input and output capacitances aren't excessive.
5. Compare your measurements with the predictions of SPICE simulation.

## 4.0 SPICE Analysis

### 4.1 Spice Analysis

1. Construct the SPICE deck for the experiments performed in section 3. You will see that the poles don't agree exactly with the values measured. Can you think of reasons why? *Hint*: consider the effect of large parasitic capacitances external to the transistor, such as the board and cable capacitances.
2. Include in your SPICE deck the parasitic capacitances that you thought of in part 1 and repeat the analysis. Do the lab measurements agree better with your SPICE results?