Lecture 15

OUTLINE

- MOSFET structure & operation (qualitative)
- Review of electrostatics
- The (N)MOS capacitor
  - Electrostatics
  - Charge vs. voltage characteristic

- Reading: Chapter 6.1-6.2.1

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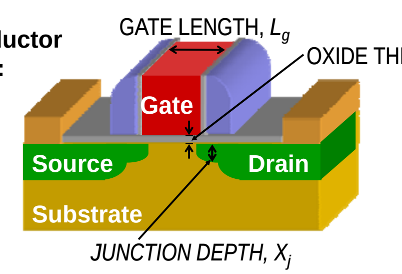
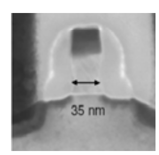
The MOSFET

Metal-Oxide-Semiconductor Field-Effect Transistor:

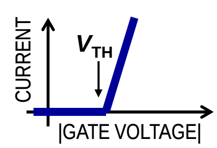




M. Bohr, *Intel Developer Forum*, September 2004

- Current flowing through the **channel** between the **source** and **drain** is controlled by the **gate** voltage.

- **"N-channel" & "P-channel" MOSFETs operate in a complementary manner**
  "CMOS" = Complementary MOS



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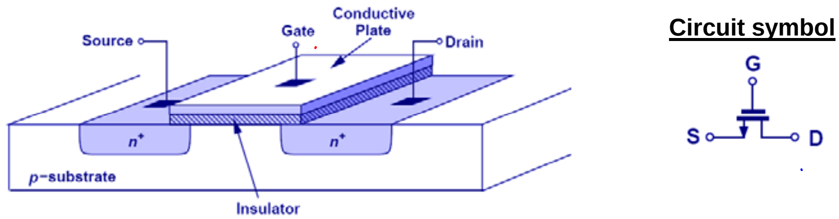
N-Channel MOSFET Structure



- The conventional gate material is heavily doped polycrystalline silicon (referred to as "polysilicon" or "poly-Si" or "poly")
  - Note that the gate is usually doped the same type as the source/drain, *i.e.* the gate and the substrate are of opposite types.
- The conventional gate insulator material is SiO_2.
- To minimize current flow between the substrate (or "body") and the source/drain regions, the p-type substrate is grounded.

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Review: Charge in a Semiconductor

- Negative charges:
  - Conduction electrons (density = n)
  - Ionized acceptor atoms (density = N_A)
- Positive charges:
  - Holes (density = p)
  - Ionized donor atoms (density = N_D)
- The ***net charge density*** [C/cm^3] in a semiconductor is

$$\rho = q(p - n + N_D - N_A)$$

- Note that p, n, N_D, and N_A each can vary with position.
- The mobile carrier concentrations (n and p) in the channel of a MOSFET can be modulated by an electric field via V_G.

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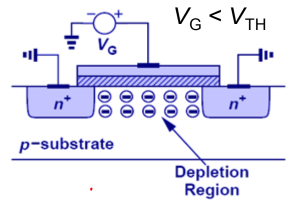
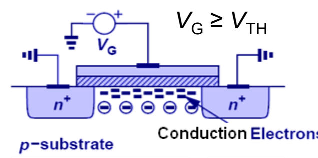
Channel Formation (Qualitative)

- As the gate voltage (V_G) is increased, holes are repelled away from the substrate surface.
  - The surface is depleted of mobile carriers. The charge density within the ***depletion region*** is determined by the dopant ion density.



- As V_G increases above the **threshold voltage** $\boldsymbol{V_{TH}}$, a layer of conduction electrons forms at the substrate surface.
  - For $V_G > V_{TH}$, $n > N_A$ at the surface.
  - → **The surface region is "inverted" to be n-type.**



The electron ***inversion layer*** serves as a resistive path (***channel***) for current to flow between the heavily doped (*i.e.* highly conductive) ***source*** and ***drain*** regions.

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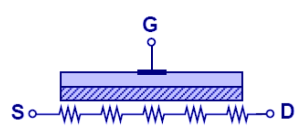
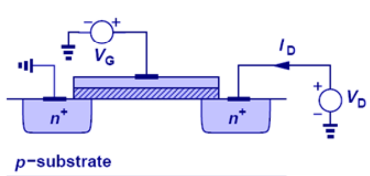
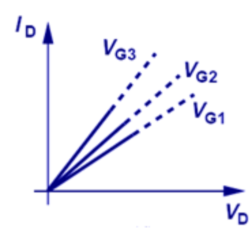
Voltage-Dependent Resistor

- In the ON state, the MOSFET channel can be viewed as a resistor.



- Since the mobile charge density within the channel depends on the gate voltage, the channel resistance is voltage-dependent.





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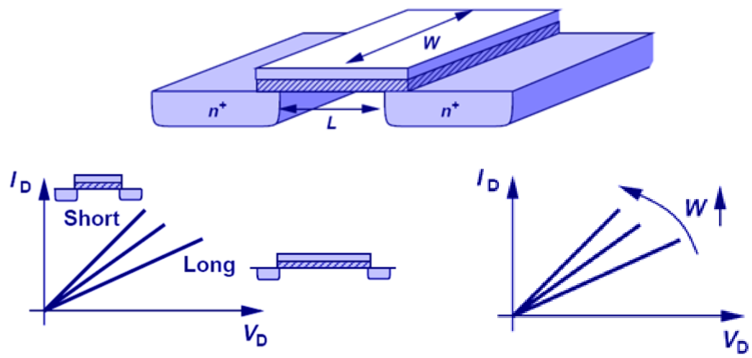
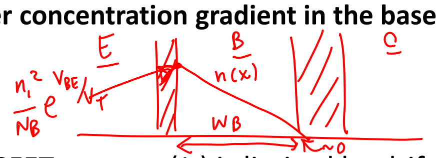
Channel Length & Width Dependence

- Shorter channel length and wider channel width each yield lower channel resistance, hence larger drain current.
  - Increasing *W* also increases the gate capacitance, however, which limits circuit operating speed (frequency).



Comparison: BJT *vs.* MOSFET

- In a BJT, current (I_C) is limited by diffusion of carriers from the emitter to the collector.
  - I_C increases exponentially with input voltage (V_{BE}), because the **carrier concentration gradient in the base** is proportional to e^{V_{BE}/V_T}

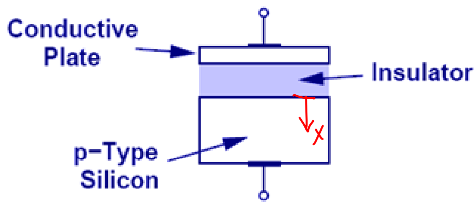


- In a MOSFET, current (I_D) is limited by drift of carriers from the source to the drain.
  - I_D increases ~linearly with input voltage (V_G), because the **carrier concentration in the channel** is proportional to (V_G-V_{TH})

In order to understand how MOSFET design parameters affect MOSFET performance, we first need to understand how a MOS capacitor works...

MOS Capacitor

- A metal-oxide-semiconductor structure can be considered as a parallel-plate capacitor, with the top plate being the positive plate, the gate insulator being the dielectric, and the p-type semiconductor substrate being the negative plate.



- The negative charges in the semiconductor (for $V_G > 0$) are comprised of conduction electrons and/or acceptor ions.

In order to understand how the potential and charge distributions within the Si depend on V_G, we need to be familiar with electrostatics...

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Gauss' Law

$$\nabla \cdot E = \frac{\rho}{\varepsilon}$$

ρ is the net charge density

ε is the dielectric permittivity

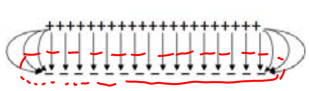
→ If the magnitude of electric field changes, there must be charge!

- **In a charge-free region, the electric field must be constant.**

- Gauss' Law equivalently says that if there is a *net* electric field leaving a region, there must be positive charge in that region:

$$\iiint_V \nabla \cdot E\, dV = \iiint_V \frac{\rho}{\varepsilon} dV$$

$$\oint_V \nabla \cdot E\, dV = \oint_S E \cdot dS \qquad \oint_V \frac{\rho}{\varepsilon} dV = \frac{Q}{\varepsilon}$$



$$\oint E \cdot dS = \frac{Q}{\varepsilon}$$

The integral of the electric field over a closed surface is proportional to the charge within the enclosed volume

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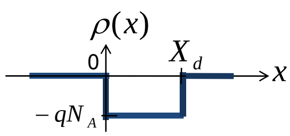
Gauss' Law in 1-D

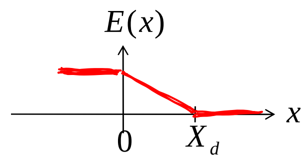
$$\nabla \cdot E = \frac{dE}{dx} = \frac{\rho}{\varepsilon}$$

$$dE = \frac{\rho}{\varepsilon} dx$$

$$E(x) = E(x_0) + \int_{x_0}^{x} \frac{\rho(x')}{\varepsilon} dx'$$

- Consider a pulse charge distribution:





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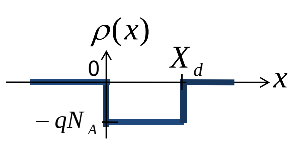
Electrostatic Potential

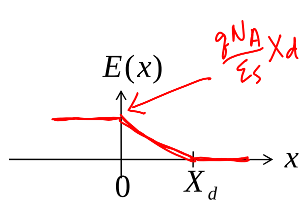
- The electric field (force) is related to the potential (energy):

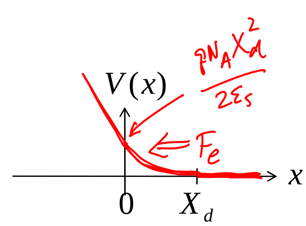
$$E = -\frac{dV}{dx} \quad \Rightarrow \quad \frac{d^2V(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon}$$

  – Note that an electron (–*q* charge) drifts in the direction of increasing potential:

$$F_e = -qE = -q\frac{dV}{dx}$$







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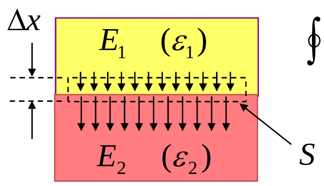
Boundary Conditions

- **Electrostatic potential must be a continuous function.** Otherwise, the electric field (force) would be infinite.
- Electric field does not have to be continuous, however. Consider an interface between two materials:



$$\oint \varepsilon E \cdot dS = -\varepsilon_1 E_1 S + \varepsilon_2 E_2 S = Q_{inside}$$

$$\text{If } \; Q_{inside} \xrightarrow[\Delta x \to 0]{} 0, \text{ then}$$

$$-\varepsilon_1 E_1 S + \varepsilon_2 E_2 S = 0$$

$$\frac{E_1}{E_2} = \frac{\varepsilon_2}{\varepsilon_1}$$

Discontinuity in electric displacement εE → charge density at interface!

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MOS Capacitor Electrostatics

- **Gate electrode:**
  - Since $E(x) = 0$ in a metallic material, ***V*(*x*) is constant**.
- **Gate-electrode/gate-insulator interface:**
  - The gate charge is located at this interface.

  → $E(x)$ changes to a non-zero value inside the gate insulator.
- **Gate insulator:**
  - Ideally, there are no charges within the gate insulator.

  → $E(x)$ is constant, and ***V*(*x*) is linear**.
- **Gate-insulator/semiconductor interface:**
  - Since the dielectric permittivity of SiO_2 is lower than that of Si, $E(x)$ is larger in the gate insulator than in the Si.
- **Semiconductor:**
  - If $\rho(x)$ is constant (non-zero), then ***V*(*x*) is quadratic**.

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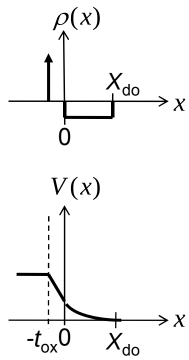
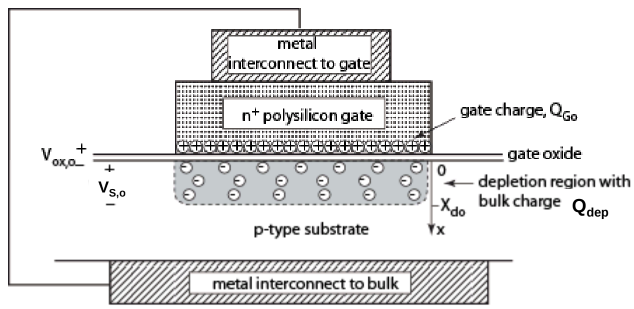
MOS Capacitor: V_{GB} = 0

- If the gate and substrate materials are not the same (typically the case), there is a built-in potential (~1V across the gate insulator).
  - Positive charge is located at the gate interface, and negative charge in the Si.
  - The substrate surface region is depleted of holes, down to a depth X_{do}





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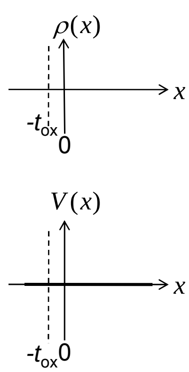
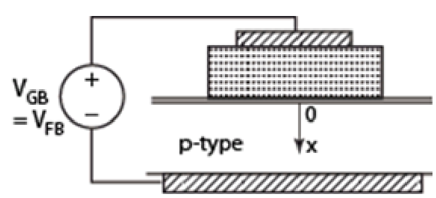
Flatband Voltage, V_{FB}

- The built-in potential can be "cancelled out" by applying a gate voltage that is equal in magnitude (but of the opposite polarity) as the built-in potential. This gate voltage is called the ***flatband voltage*** because the resulting potential profile is flat.





There is no net charge (*i.e.* $\rho(x)$=0) in the semiconductor under for $V_{GB} = V_{FB}$.

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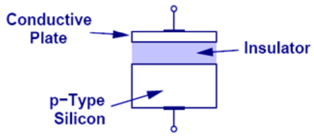
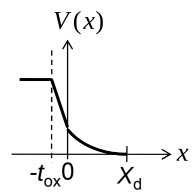
Voltage Drops across a MOS Capacitor

$$V_{GB} - V_{FB} = V_{ox} + V_S$$





- If we know the total charge within the semiconductor (Q'_S) , we can find the electric field within the gate insulator (E_{ox}) and hence the voltage drop across the gate insulator (V_{ox}):

$$\oint E \cdot dS = E_{ox} A = \frac{-Q'_S}{\varepsilon_{ox}} \qquad V_{ox} = E_{ox} t_{ox} = \left(\frac{-Q'_S}{A\varepsilon_{ox}} \right) t_{ox} = \frac{-Q_S}{C_{ox}}$$

where Q_S is the areal charge density in the semiconductor [C/cm^2]

and $C_{ox} \equiv \varepsilon_{ox} / t_{ox}$ is the areal gate capacitance [F/cm^2]

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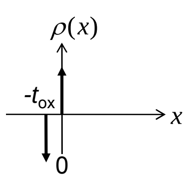
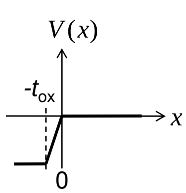
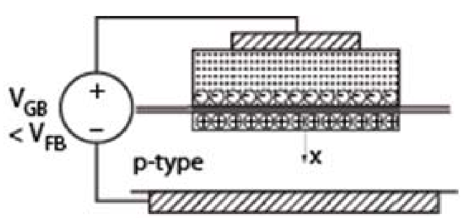
$V_{GB} < V_{FB}$ (Accumulation)

- If a gate voltage more negative than V_{FB} is applied, then holes will accumulate at the gate-insulator/semiconductor interface.







Areal gate charge density [C/cm^2]:

$$Q_G = C_{ox} \cdot (V_{GB} - V_{FB})$$

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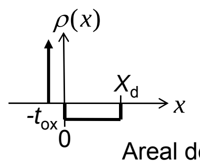
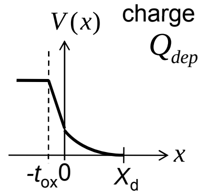
$V_{FB} < V_{GB} < V_{TH}$ (Depletion)

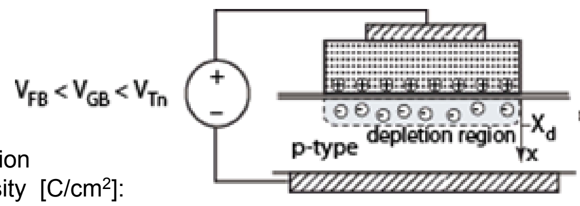
- If the applied gate voltage is greater than V_{FB}, then the semiconductor surface will be depleted of holes.
  - If the applied gate voltage is less than V_{TH}, the concentration of conduction electrons at the surface is smaller than N_A → $\rho(x) \cong -qN_A(x)$





Areal depletion charge density [C/cm²]:

$$Q_{dep} = -qN_A X_d$$



$$V_{GB} - V_{FB} = V_{ox} + V_B = \frac{qN_A X_d}{C_{ox}} + \frac{qN_A X_d^2}{2\varepsilon_{Si}}$$

$$\Rightarrow X_d = \frac{\varepsilon_{Si}}{C_{ox}}\left[\sqrt{1 + \frac{2C_{ox}^2 (V_{GB} - V_{FB})}{q\varepsilon_{Si} N_A}} - 1\right]$$

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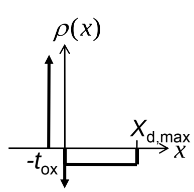
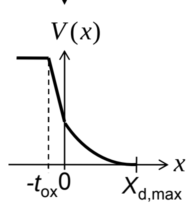
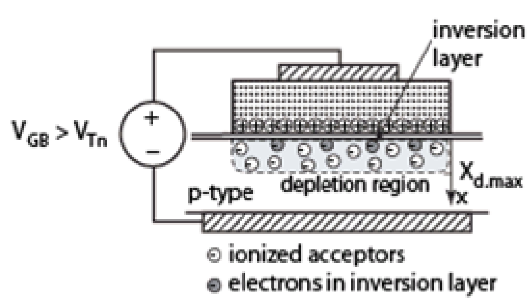
$V_{GB} > V_{TH}$ (Inversion)

- If the applied gate voltage is greater than V_{TH}, then $n > N_A$ at the semiconductor surface.
  - At $V_{GB} = V_{TH}$, the total potential dropped in the Si is $2\phi_B$ where $\phi_B = V_T \ln\left(\frac{N_A}{n_i}\right)$







$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{2q\varepsilon_{Si} N_A (2\phi_B)}}{C_{ox}}$$

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Maximum Depletion Depth, $X_{d,max}$

- As V_{GB} is increased above V_{TH}, V_S and hence the depth of the depletion region (X_d) increases very slowly.
  - This is because n increases exponentially with V_S, whereas X_d increases with the square root of V_S. Thus, most of the incremental negative charge in the semiconductor comes from additional conduction electrons rather than additional ionized acceptor atoms, when n exceeds N_A.

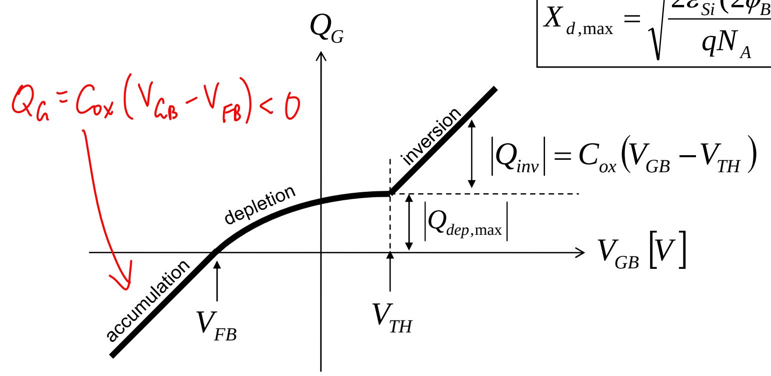
→ X_d can be reasonably approximated to reach a maximum value ($X_{d,max}$) for $V_{GB} \geq V_{TH}$.
  - Q_{dep} thus reaches a maximum of $Q_{dep,max}$ at $V_{GB} = V_{TH}$.

- If we assume that only the inversion-layer charge increases with increasing V_{GB} above V_{TH}, then

$$Q_{inv} = -C_{ox}(V_{GB} - V_{TH}) \text{ and so } Q_G(V_{GB}) = C_{ox}(V_{GB} - V_{TH}) + Q_{dep,\max}$$

Q-V Curve for MOS Capacitor

$$X_{d,\max} = \sqrt{\frac{2\varepsilon_{Si}(2\phi_B)}{qN_A}}$$



$$Q_{dep,\max} = -qN_A X_{d,\max} = -\sqrt{2qN_A\varepsilon_{Si}(2\varphi_B)}$$