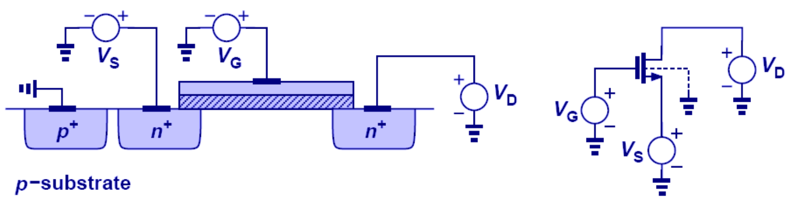
Lecture 17

OUTLINE

- NMOSFET in ON state (cont'd)
  - Body effect
  - Channel-length modulation
  - Velocity saturation
- NMOSFET in OFF state
- MOSFET models
- PMOSFET

- Reading: Finish Chap. 6

Body Effect Example



$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\varphi_B + V_{SB}} - \sqrt{2\varphi_B}\right)$$

where $\gamma = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{ox}}$

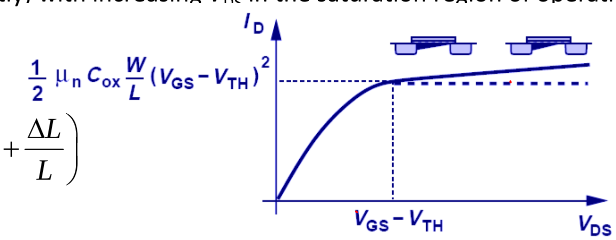
Example:
Typical values
$\gamma \sim 0.5$
$\varphi_B = 0.48\text{V}$ for $N_A = 10^{18}\text{cm}^{-3}$
(substrate doping)
A substrate bias of $V_{SB} = 1\text{V}$
produce a V_{TH} shift of 0.2V

Channel-Length Modulation

- The pinch-off point moves toward the source as V_{DS} increases.

→ The length of the inversion-layer channel becomes shorter with increasing V_{DS}.

→ I_D increases (slightly) with increasing V_{DS} in the saturation region of operation.



$$I_{Dsat} \propto \frac{1}{L-\Delta L} \cong \frac{1}{L}\left(1+\frac{\Delta L}{L}\right)$$

$$\Delta L \propto \left(V_{DS} - V_{DSsat}\right)$$

$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2\left[1+\lambda\left(V_{DS}-V_{D,sat}\right)\right]$$

λ: channel length modulation coefficient

* Note: in Razavi: $I_{D,sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2\left[1+\lambda V_{DS}\right]$

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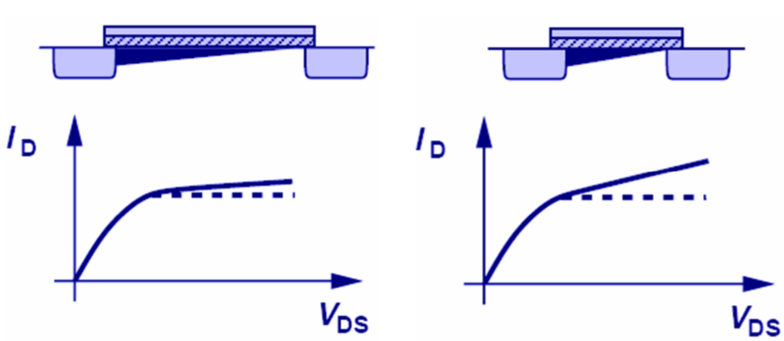
λ and L

- The effect of channel-length modulation is less for a long-channel MOSFET than for a short-channel MOSFET.

$$\lambda \propto \frac{1}{L} \quad \Rightarrow \quad \text{short channel MOSFET has larger } \lambda$$



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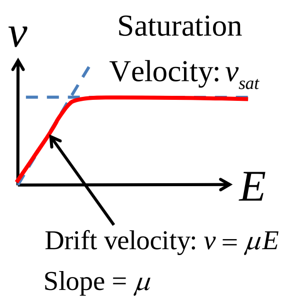
Velocity Saturation

- In state-of-the-art MOSFETs, the channel is very short (<0.1μm); hence the lateral electric field is very high and carrier drift velocities can reach their saturation levels.
  - The electric field magnitude at which the carrier velocity saturates is $\boldsymbol{E_{sat}}$.



$$v_{sat} = \begin{cases} 8\times10^{6} \text{ cm/s for electrons in Si} \\ 6\times10^{6} \text{ cm/s for holes in Si} \end{cases}$$

$$\begin{cases} \text{NMOS: } \mu_n \approx 250 \text{ cm}^2\text{/V-s} \Rightarrow E_{sat} \approx 30,000 \text{ V/cm} \\ \text{PMOS: } \mu_n \approx 80 \text{ cm}^2\text{/V-s} \Rightarrow E_{sat} \approx 80,000 \text{ V/cm} \end{cases}$$

For $L = 0.1\ \mu\text{m}$

$$\begin{cases} V_{D,sat} = 0.3 \text{ V for NMOS} \\ V_{D,sat} = 0.8 \text{ V for PMOS} \end{cases}$$

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Impact of Velocity Saturation

- Recall that $I_D = WQ_{inv}(y)v(y)$

- If $V_{DS} > E_{sat} \times L$, the carrier velocity will saturate and hence the drain current will saturate:

$$I_{D,sat} = WQ_{inv}v_{sat} = WC_{ox}(V_{GS} - V_{TH})v_{sat}$$

  - **$I_{D,sat}$ is proportional to $V_{GS} - V_{TH}$ rather than $(V_{GS} - V_{TH})^2$**
  - **$I_{D,sat}$ is not dependent on L**
  - **$I_{D,sat}$ is dependent on W**

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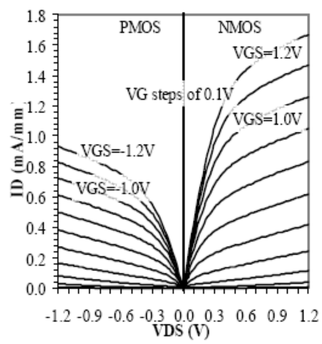
Short-Channel MOSFET I_D-V_{DS}



I_{DS}-V_{DS} for 35nm gate lengths

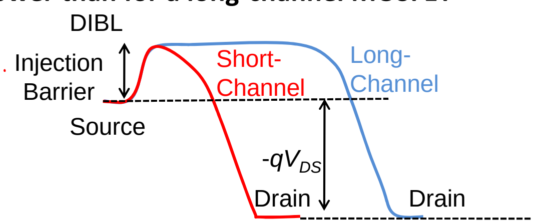
P. Bai et al. (Intel Corp.), *Int'l Electron Devices Meeting*, 2004.

- $I_{D,sat}$ is proportional to V_{GS}-V_{TH} rather than $(V_{GS}$-$V_{TH})^2$
- $V_{D,sat}$ is smaller than V_{GS}-V_{TH}
- Channel-length modulation is apparent (?)

Drain Induced Barrier Lowering (DIBL)

- In a **short-channel MOSFET**, the source & drain regions each "support" a significant fraction of the total channel depletion charge Q_{dep}×W×L

  → **V_{TH} is lower than for a long-channel MOSFET**



- As the drain voltage increases, the reverse bias on the body-drain PN junction increases, and hence the drain depletion region widens.

  → V_{TH} decreases with increasing drain bias.

  (The barrier to carrier diffusion from the source into the channel is reduced.)

  → **I_D increases with increasing drain bias.**

NMOSFET in OFF State

- We had previously assumed that there is no channel current when $V_{GS} < V_{TH}$. This is incorrect!
- As V_{GS} is reduced below V_{TH} (towards 0 V), the potential barrier to carrier diffusion from the source into the channel is increased. ***I_D* becomes limited by carrier diffusion** into the channel, rather than by carrier drift through the channel.

  (This is similar to the case of a PN junction diode!)

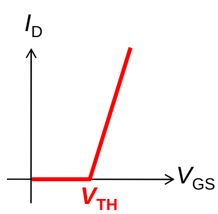
  → I_D varies exponentially with the potential barrier height at the source, which varies directly with the channel potential.

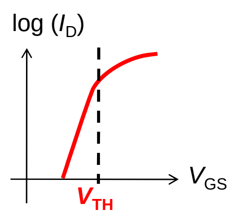
Sub-Threshold Leakage Current

- Recall that, in the depletion (sub-threshold) region of operation, the channel potential is capacitively coupled to the gate potential. A change in gate voltage (ΔV_{GS}) results in a change in channel voltage (ΔV_{CS}):

$$\Delta V_{CS} = \Delta V_{GS} \times \left(\frac{C_{ox}}{C_{ox} + C_{dep}} \right) \equiv \Delta V_{GS} / m \quad ; \quad m = 1 + \frac{C_{dep}}{C_{ox}} > 1$$

- Therefore, the sub-threshold current ($I_{D,subth}$) decreases exponentially with linearly decreasing V_{GS}/m



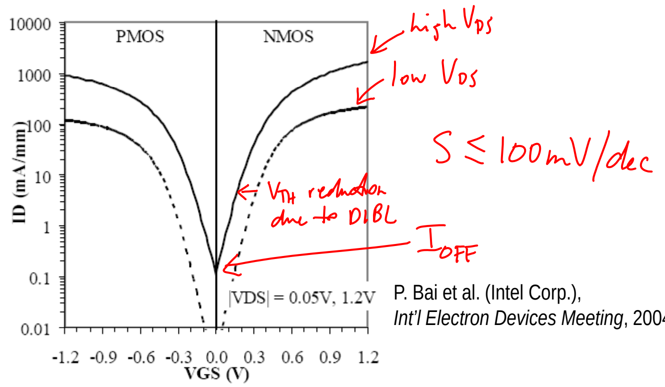


Sub-threshold swing:

$$S \equiv \left(\frac{d(\log_{10} I_{DS})}{dV_{GS}} \right)^{-1}$$

$$S = mV_T \ln(10) > 60\text{mV/dec}$$

Short-Channel MOSFET I_D-V_{GS}



P. Bai et al. (Intel Corp.), *Int'l Electron Devices Meeting*, 2004.

Sub-threshold curves (I_{DS}-V_{GS}) for 35nm gate lengths

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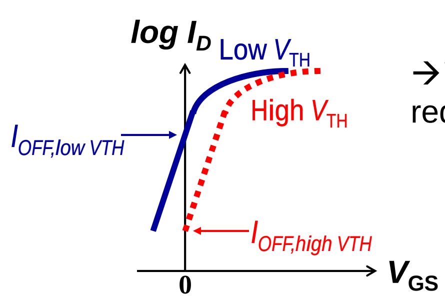
V_{TH} Design Trade-Off

- Low V_{TH} is desirable for high ON-state current:

$$I_{D,sat} \propto (V_{DD} - V_{TH})^{\eta} \qquad 1 < \eta < 2$$

- But high V_{TH} is needed for low OFF-state current:



→ V_{TH} cannot be reduced aggressively.

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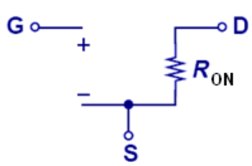
MOSFET Large-Signal Models ($V_{GS} > V_{TH}$)

- Depending on the value of V_{DS}, the MOSFET can be represented with different large-signal models.

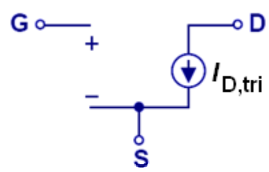
Triode Region | **Saturation Region**

$V_{DS} << 2(V_{GS}-V_{TH})$



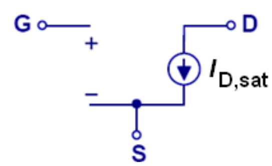
$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$

$V_{DS} < V_{D,sat}$



$$I_{D,tri} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH}) - \frac{V_{DS}}{2}\right] V_{DS}$$

$V_{DS} > V_{D,sat}$



$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 \left[1 + \lambda(V_{DS} - V_{D,sat})\right]$$

or

$$I_{D,sat} = v_{sat} W C_{ox} (V_{GS} - V_{TH})\left[1 + \lambda(V_{DS} - V_{D,sat})\right]$$

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MOSFET Transconductance, g_m

- Transconductance (g_m) is a measure of how much the drain current changes when the gate voltage changes.

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}}$$

- For amplifier applications, the MOSFET is usually operating in the saturation region.
  - **For a long-channel MOSFET:**

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})\left\{1 + \lambda\left(V_{DS} - V_{D,sat}\right)\right\} = \frac{2 I_D}{V_{GS} - V_{TH}}$$

  - **For a short-channel MOSFET:**

$$g_m = v_{sat} W C_{ox}\left\{1 + \lambda\left(V_{DS} - V_{D,sat}\right)\right\} = \frac{I_D}{V_{GS} - V_{TH}}$$

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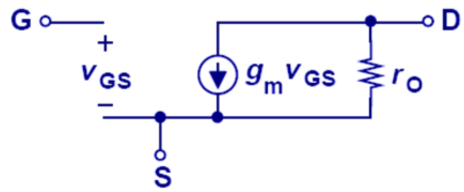
MOSFET Small-Signal Model

(Saturation Region of Operation)

- The effect of channel-length modulation or DIBL (which cause I_D to increase linearly with V_{DS}) is modeled by the transistor output resistance, r_o.



$$r_o \equiv \frac{\partial V_{DS}}{\partial I_D} \approx \frac{1}{\lambda I_D}$$

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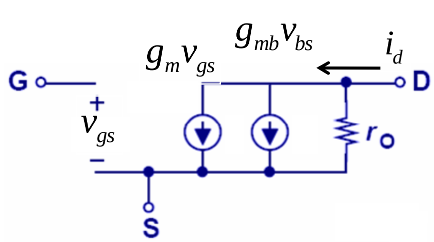
Derivation of Small-Signal Model

(Long-Channel MOSFET, Saturation Region)

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2\left[1+\lambda\left(V_{DS}-V_{D,sat}\right)\right]$$

$$i_d = \frac{\partial I_D}{\partial V_{GS}}v_{gs} + \frac{\partial I_D}{\partial V_{BS}}v_{bs} + \frac{\partial I_D}{\partial V_{DS}}v_{ds} \equiv g_m v_{gs} + g_{mb}v_{bs} + \frac{1}{r_o}v_{ds}$$



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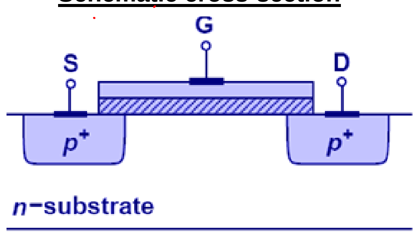
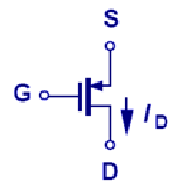
PMOS Transistor

- A p-channel MOSFET behaves similarly to an n-channel MOSFET, except the polarities for I_D and V_{GS} are reversed.

Schematic cross-section



Circuit symbol



- The small-signal model for a PMOSFET is the same as that for an NMOSFET.
  – The values of g_m and r_o will be different for a PMOSFET *vs.* an NMOSFET, since mobility & saturation velocity are different for holes *vs*. electrons.

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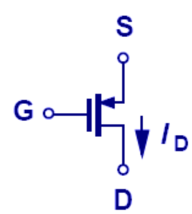
PMOS *I-V* Equations

$$I_{D,tri} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[2\left(V_{SG}-V_{TH}\right)V_{DS}-V_{DS}^2\right] \qquad DS\leftrightarrow SD \quad GS\leftrightarrow SG$$

$$= \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[2\left(\left|V_{GS}\right|-\left|V_{TH}\right|\right)\left|V_{DS}\right|-V_{DS}^2\right]$$



Long Channel:

$$I_{D,sat} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(V_{SG}-V_{TH}\right)^2\left[1+\lambda\left(V_{SD}-V_{SD,sat}\right)\right]$$

$$= \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(\left|V_{GS}\right|-\left|V_{TH}\right|\right)^2\left[1+\lambda\left(\left|V_{DS}\right|-\left|V_{D,sat}\right|\right)\right]$$

Short Channel:

$$I_{D,sat} = v_{sat}WC_{ox}\left(V_{SG}-V_{TH}\right)\left[1+\lambda\left(V_{SD}-V_{SD,sat}\right)\right]$$

$$= v_{sat}WC_{ox}\left(\left|V_{SG}\right|-\left|V_{TH}\right|\right)\left[1+\lambda\left(\left|V_{DS}\right|-\left|V_{D,sat}\right|\right)\right]$$

Note: $V_{GS}<0, V_{DS}<0, V_{D,sat}<0, V_{TH}<0$ in PMOS

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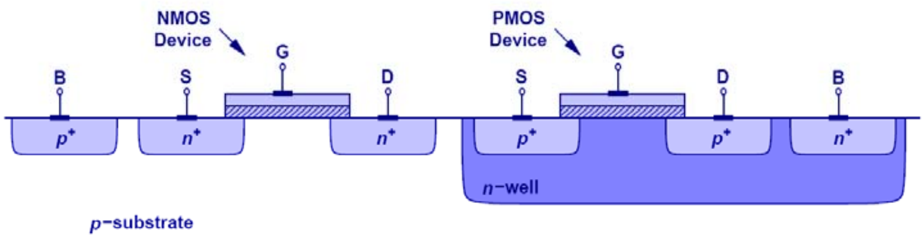
CMOS Technology

- It possible to form deep n-type regions ("well") within a p-type substrate to allow PMOSFETs and NMOSFETs to be co-fabricated on a single substrate.
- This is referred to as CMOS ("Complementary MOS") technology.

Schematic cross-section of CMOS devices



Comparison of BJT and MOSFET

- The BJT can achieve much higher g_m than a MOSFET, for a given bias current, due to its exponential *I-V* characteristic.

	(Long-Channel)
Bipolar Transistor	MOSFET
Exponential Characteristic	Quadratic Characteristic
Active: $V_{CB} > 0$	Saturation: $V_{DS} > V_{GS} - V_{TH}$
Saturation: $V_{CB} < 0$	Triode: $V_{DS} < V_{GS} - V_{TH}$
Finite Base Current	Zero Gate Current
Early Effect	Channel−Length Modulation
Diffusion Current	Drift Current
−	Voltage−Dependent Resistor

(Short-Channel)

MOSFET

Linear

$V_{GS} > V_{Dsat}$; $V_{Dsat} = E_{sat}L$

$V_{GS} < V_{Dsat}$