## Lecture 18

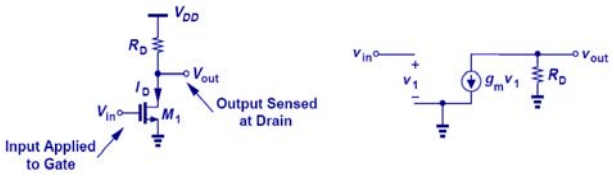
**OUTLINE**

- Basic MOSFET amplifier
- MOSFET biasing
- MOSFET current sources
- Common-source amplifier

- Reading: Chap. 7.1-7.2



## Common-Source Stage



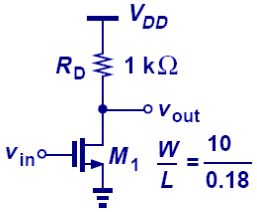

$$\lambda = 0$$

$$A_v = -g_m R_D$$

$$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D R_D}$$



## Operation in Saturation




Condition for $M_1$ in saturation

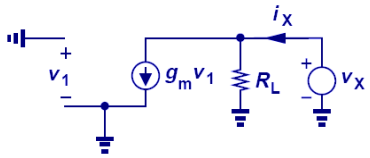
$$V_{out} > V_{in} - V_{TH}$$

$$\Rightarrow V_{DD} - R_D I_D > (V_{GS} - V_{TH})$$

- In order to maintain operation in saturation, $V_{out}$ cannot fall below $V_{in}$ by more than one threshold voltage.
- The condition above ensures operation in saturation.



## CS Stage with λ=0

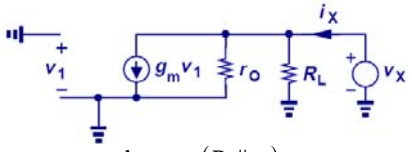



$$A_v = -g_m R_L$$

$$R_{in} = \infty$$

$$R_{out} = R_L$$

## CS Stage with $\lambda \neq 0$

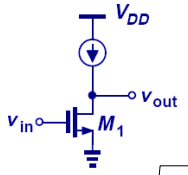


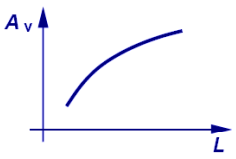

$$A_v = -g_m(R_L \| r_O)$$
$$R_{in} = \infty$$
$$R_{out} = R_L \| r_O$$

- However, channel length modulation leads to finite output resistance, $r_o$, which is in parallel with the load resistance, $R_L$



## CS Gain Variation with Channel Length



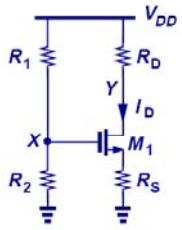




$$|A_v| = \frac{\sqrt{2\mu_n C_{ox}\frac{W}{L}}}{\lambda\sqrt{I_D}} \propto \sqrt{\frac{2\mu_n C_{ox} WL}{I_D}}$$

- Since $\lambda$ is inversely proportional to L, the intrinsic voltage gain actually becomes proportional to the square root of L.



## MOS Biasing




$$\frac{R_1}{R_1+R_2}V_{DD} = V_{GS} + I_D R_S$$
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

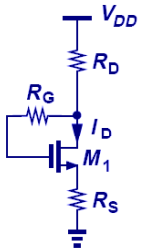
2 unknows ($V_{GS}$, $I_D$), 2 equations $\Rightarrow$

$$V_{GS} = -(V_1 - V_{TH}) + \sqrt{V_1^2 + 2V_1\left(\frac{R_2 V_{DD}}{R_1+R_2} - V_{TH}\right)}$$
$$V_1 = \frac{1}{\mu_n C_{ox}\frac{W}{L}R_S}$$

- Voltage at X is determined by $V_{DD}$, $R_1$, and $R_2$.
- $V_{GS}$ can be found using the equation above, and $I_D$ can be found by using the NMOS current equation.



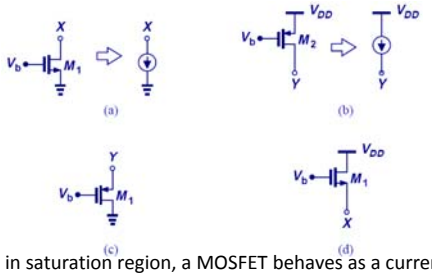
## Self-Biased MOS Stage




$$I_D R_D + V_{GS} + R_S I_D = V_{DD}$$
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

- The circuit above is analyzed by noting $M_1$ is in saturation and no potential drop appears across RG.

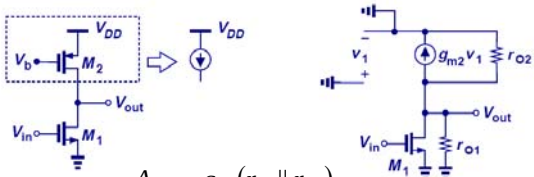
## Current Sources




- When in saturation region, a MOSFET behaves as a current source.
- NMOS draws current from a point to ground (sinks current), whereas PMOS draws current from $V_{DD}$ to a point (sources current).



## CS Stage with Current-Source Load



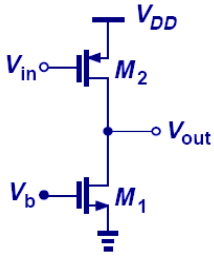

$$A_v = -g_{m1}(r_{O1} \| r_{O2})$$

$$R_{out} = r_{O1} \| r_{O2}$$

- To alleviate the headroom problem, an active current-source load is used.
- This is advantageous because a current-source has a high output resistance and can tolerate a small voltage drop across it.



## PMOS CS Stage with NMOS as Load

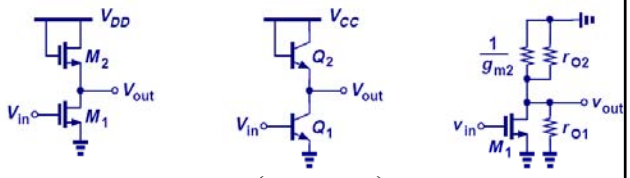



$$A_v = -g_{m2}(r_{O1} \| r_{O2})$$

- Similarly, with PMOS as input stage and NMOS as the load, the voltage gain is the same as before.



## CS Stage with Diode-Connected Load

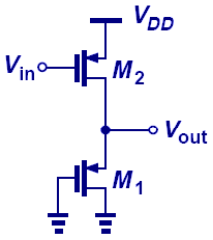



$$A_v = -g_{m1}\left(\frac{1}{g_{m2}} \| r_{O2} \| r_{O1}\right)$$

$$A_v = -g_{m1} \cdot \frac{1}{g_{m2}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

- Lower gain, but less dependent on process parameters.

## CS Stage with Diode-Connected PMOS Device

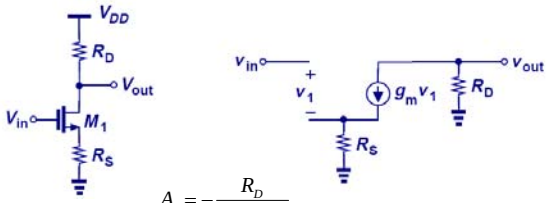



$$A_v = -g_{m2}\left(\frac{1}{g_{m1}} \| r_{o1} \| r_{o2}\right)$$

- Note that PMOS circuit symbol is usually drawn with the source on top of the drain.



## CS Stage with Degeneration



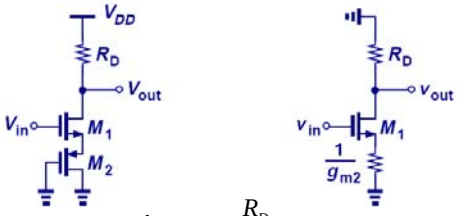

$$A_v = -\frac{R_D}{\frac{1}{g_m} + R_S}$$

$$\lambda = 0$$

- Similar to bipolar counterpart, when a CS stage is degenerated, its gain, I/O impedances, and linearity change.



## Example of CS Stage with Degeneration

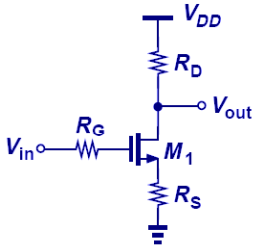



$$A_v = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

- A diode-connected device degenerates a CS stage.



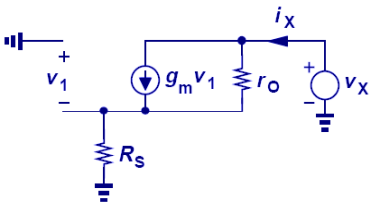
## CS Stage with Gate Resistance




$$V_{R_G} = 0$$

- Since at low frequencies, the gate conducts no current, gate resistance does not affect the gain or I/O impedances.

## Output Impedance of CS Stage with Degeneration

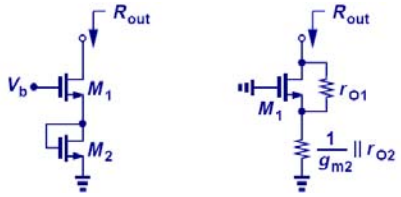



$$r_{out} \approx g_m r_O R_S + r_O$$

- Similar to the bipolar counterpart, degeneration boosts output impedance.



## Output Impedance Example (I)

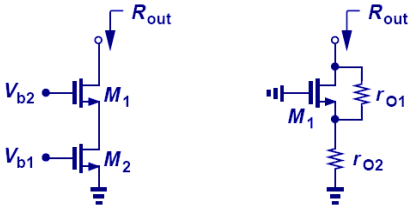



$$R_{out} = r_{O1}\left(1 + g_{m1}\frac{1}{g_{m2}}\right)$$

- When $1/g_m$ is parallel with $r_{O2}$, we often just consider $1/g_m$



## Output Impedance Example (II)

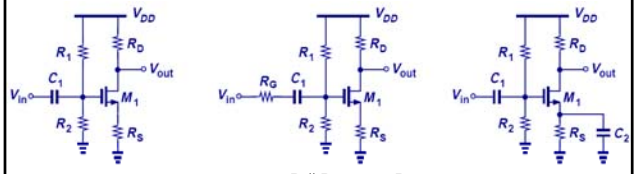



$$R_{out} \approx g_{m1} r_{O1} r_{O2} + r_{O1}$$

- In this example, the impedance that degenerates the CS stage is $r_O$, instead of $1/g_m$ in the previous example.



## CS Core with Biasing




$$A_v = \frac{R_1 \| R_2}{R_G + R_1 \| R_2} \cdot \frac{-R_D}{\frac{1}{g_m} + R_S}, \qquad A_v = -g_m R_D$$

- Degeneration is used to stabilize bias point, and a bypass capacitor can be used to obtain a larger small-signal voltage gain at the frequency of interest.