Lecture 21

OUTLINE

- Frequency Response
  - Review of basic concepts
  - high-frequency MOSFET model
  - CS stage
  - CG stage
  - Source follower
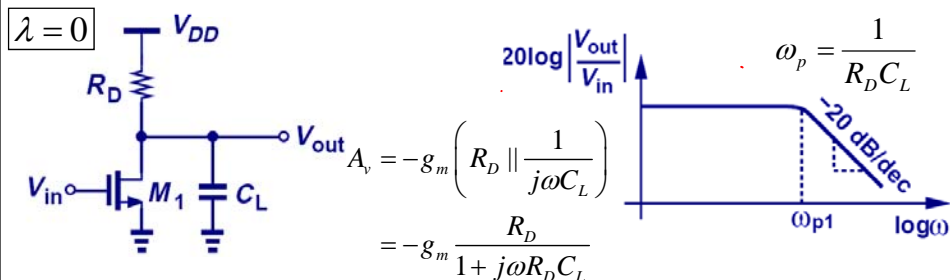 - Cascode stage

- Reading: Chapter 11

A_v Roll-Off due to C_L

- The impedance of C_L decreases at high frequencies, so that it shunts some of the output current to ground.

$$\lambda = 0$$

$$\omega_p = \frac{1}{R_D C_L}$$

$$A_v = -g_m \left(R_D \| \frac{1}{j\omega C_L} \right)$$
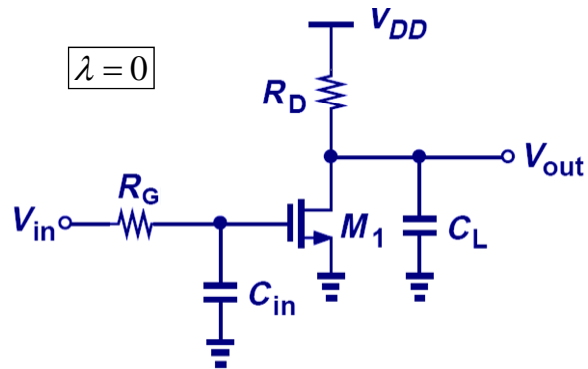
$$= -g_m \frac{R_D}{1 + j\omega R_D C_L}$$

- In general, if **node j in the signal path** has a small-signal resistance of R_j to ground and a capacitance C_j to ground, then it contributes a **pole at frequency $(R_j C_j)^{-1}$**

Pole Identification Example 1

$\lambda = 0$

V_{DD}

R_D

V_{out}

R_G

V_{in}

M_1 C_L

C_{in}

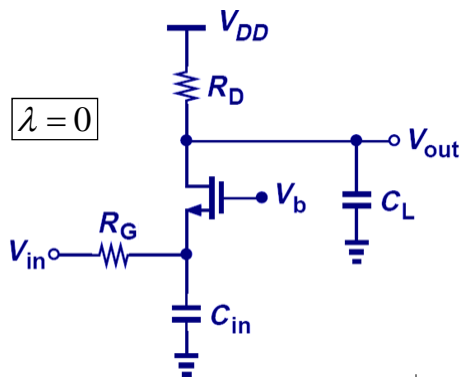$$\left|\omega_{p1}\right| = \frac{1}{R_G C_{in}}$$

$$\left|\omega_{p2}\right| = \frac{1}{R_D C_L}$$

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Pole Identification Example 2

V_{DD}

R_D

$\lambda = 0$

V_{out}

V_b C_L

R_G

V_{in}

C_{in}

$$\left|\omega_{p1}\right| = \frac{1}{\left(R_G \,\|\, \dfrac{1}{g_m}\right) C_{in}}$$

$$\left|\omega_{p2}\right| = \frac{1}{R_D C_L}$$
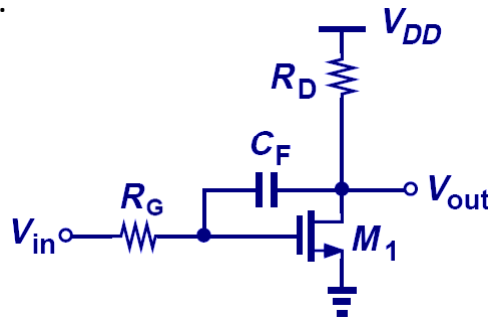
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Dealing with a Floating Capacitance

- Recall that a pole is computed by finding the resistance and capacitance between a node and (AC) GROUND.

- It is not straightforward to compute the pole due to C_F in the circuit below, because neither of its terminals is grounded.

Miller's Theorem
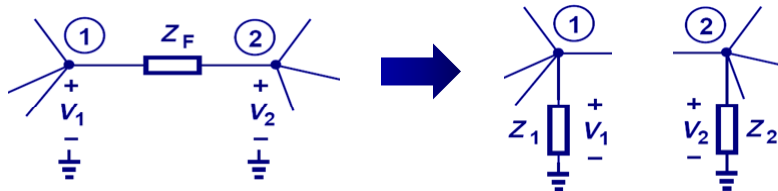
- If A_v is the voltage gain from node 1 to 2, then a floating impedance Z_F can be converted to two grounded impedances Z_1 and Z_2:

$$\frac{V_1 - V_2}{Z_F} = \frac{V_1}{Z_1} \ \Rightarrow \ Z_1 = Z_F \frac{V_1}{V_1 - V_2} = Z_F \frac{1}{1 - A_v}$$

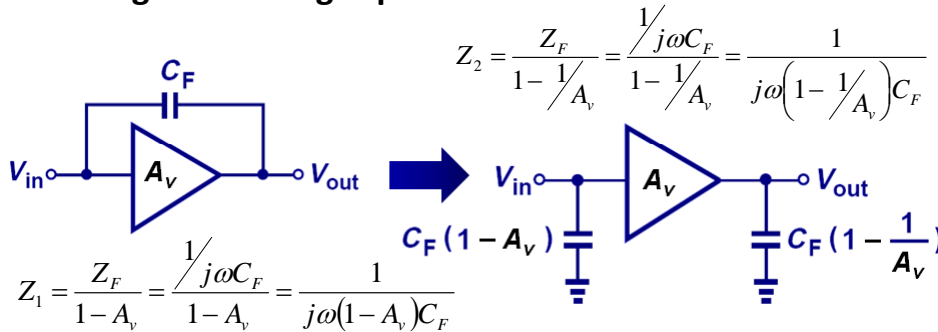$$\frac{V_1 - V_2}{Z_F} = -\frac{V_2}{Z_2} \ \Rightarrow \ Z_2 = -Z_F \frac{V_2}{V_1 - V_2} = Z_F \frac{1}{1 - \frac{1}{A_v}}$$

Miller Multiplication

- Applying Miller's theorem, we can convert a floating capacitance between the input and output nodes of an amplifier into two grounded capacitances.
- **The capacitance at the input node is larger than the original floating capacitance.**
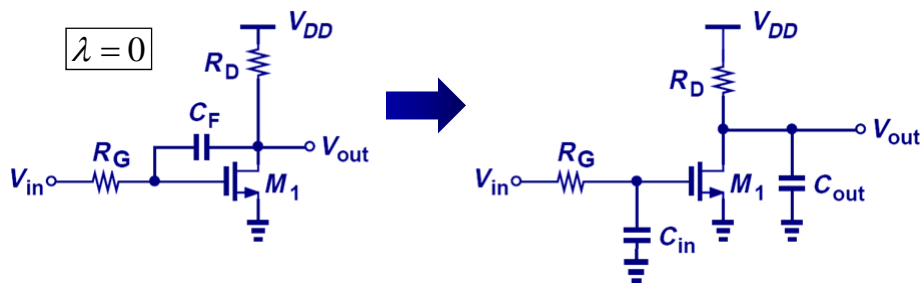
$$Z_2 = \frac{Z_F}{1 - \frac{1}{A_v}} = \frac{\frac{1}{j\omega C_F}}{1 - \frac{1}{A_v}} = \frac{1}{j\omega\left(1 - \frac{1}{A_v}\right)C_F}$$

$$Z_1 = \frac{Z_F}{1 - A_v} = \frac{\frac{1}{j\omega C_F}}{1 - A_v} = \frac{1}{j\omega(1 - A_v)C_F}$$

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Application of Miller's Theorem

$$\boxed{\lambda = 0}$$

$$\omega_{in} = \frac{1}{R_G(1 + g_m R_D)C_F}$$

$$\omega_{out} = \frac{1}{R_D\left(1 + \dfrac{1}{g_m R_D}\right)C_F}$$
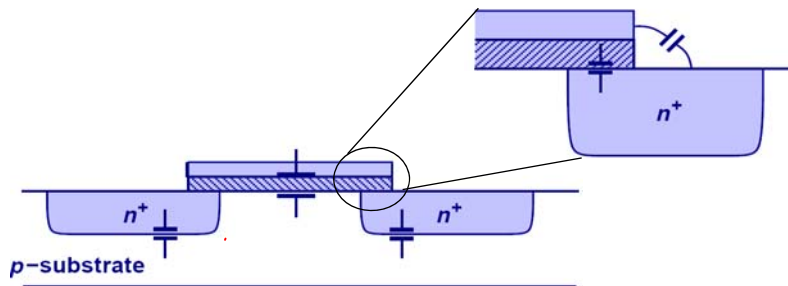
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MOSFET Intrinsic Capacitances

The MOSFET has intrinsic capacitances which affect its performance at high frequencies:

1. gate oxide capacitance between the gate and channel,
2. overlap and fringing capacitances between the gate and the source/drain regions, and
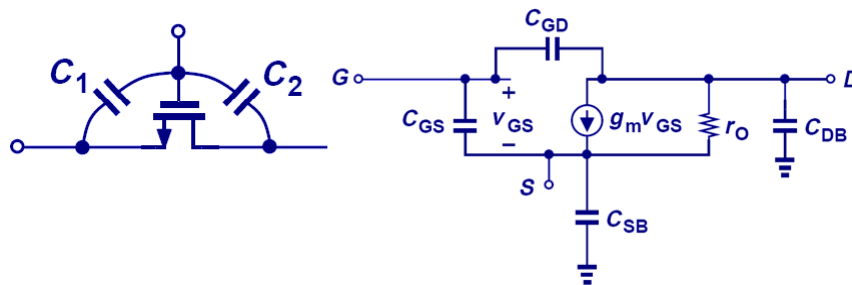3. source-bulk & drain-bulk junction capacitances (C_{SB} & C_{DB}).

High-Frequency MOSFET Model

- The gate oxide capacitance can be decomposed into a capacitance between the gate and the source (C_1) and a capacitance between the gate and the drain (C_2).

  – In saturation, $C_1 \cong (2/3) \times C_{gate}$, and $C_2 \cong 0$. ($C_{gate} = C_{ox}WL$)
  – C_1 in parallel with the source overlap/fringing capacitance → C_{GS}
  – C_2 in parallel with the drain overlap/fringing capacitance → C_{GD}

Example

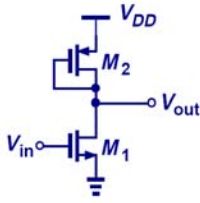| | **…with MOSFET capacitances explicitly shown** | **Simplified circuit for high-frequency analysis** |

CS stage

Transit Frequency

- The "transit" or "cut-off" frequency, f_T, is a measure of the intrinsic speed of a transistor, and is defined as the frequency where the current gain falls to 1.
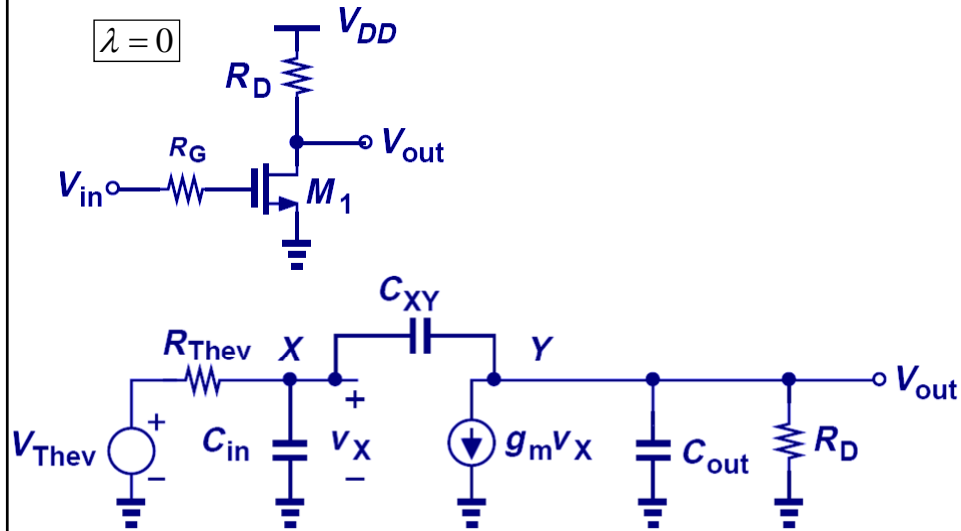
Conceptual set-up to measure f_T

$$I_{out} = g_m V_{in}$$

$$I_{in} = \frac{V_{in}}{Z_{in}}$$
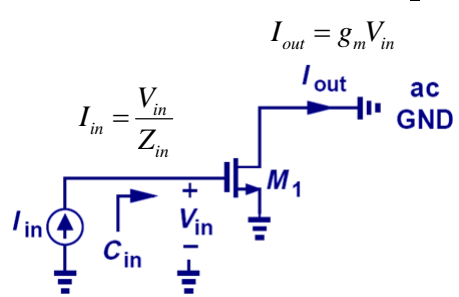
$$\left| \frac{I_{out}}{I_{in}} \right| = \left| g_m Z_{in} \right| = \left| g_m \left(\frac{1}{j\omega_T C_{in}} \right) \right| = 1$$

$$\Rightarrow \omega_T = \frac{g_m}{C_{in}}$$

$$\boxed{2\pi f_T = \frac{g_m}{C_{GS}}}$$
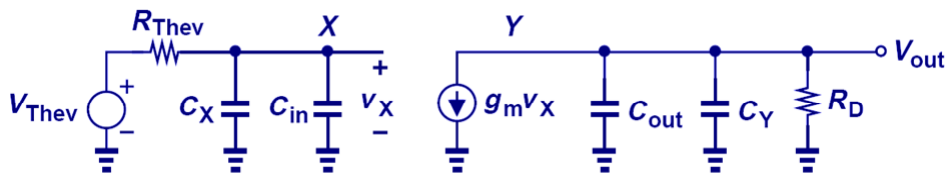
Small-Signal Model for CS Stage

$\lambda = 0$

… Applying Miller's Theorem

$V_{Thev} = V_{in}$

$R_{Thev} = R_G$

$C_X = C_{GD}(1 + g_m R_D)$

$C_Y = C_{GD}(1 + \dfrac{1}{g_m R_D})$

$$\omega_{p,in} = \frac{1}{R_{Thev}\left(C_{in} + (1 + g_m R_D)C_{GD}\right)}$$

$$\omega_{p,out} = \frac{1}{R_D\left(C_{out} + \left(1 + \dfrac{1}{g_m R_D}\right)C_{GD}\right)}$$

Note that $\omega_{p,out} > \omega_{p,in}$

Direct Analysis of CS Stage

- Direct analysis yields slightly different pole locations and an extra zero:

$$\omega_z = \frac{g_m}{C_{XY}}$$

$$\omega_{p1} = \frac{1}{(1 + g_m R_D) C_{XY} R_{Thev} + R_{Thev} C_{in} + R_D (C_{XY} + C_{out})}$$

$$\omega_{p2} = \frac{(1 + g_m R_D) C_{XY} R_{Thev} + R_{Thev} C_{in} + R_D (C_{XY} + C_{out})}{R_{Thev} R_D (C_{in} C_{XY} + C_{out} C_{XY} + C_{in} C_{out})}$$
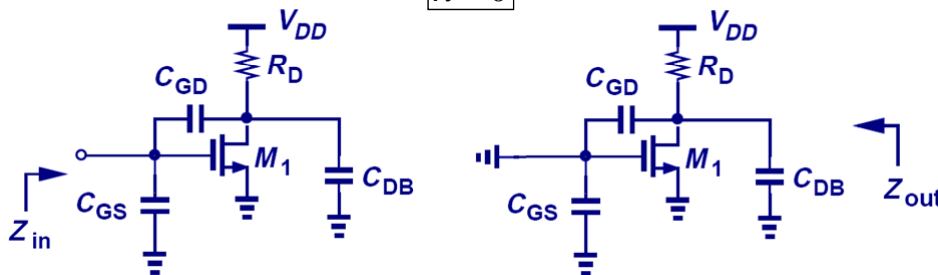
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I/O Impedances of CS Stage

$$\lambda = 0$$

$$Z_{in} \approx \frac{1}{j\omega [C_{GS} + (1 + g_m R_D) C_{GD}]} \qquad Z_{out} = \frac{1}{j\omega [C_{GD} + C_{DB}]} \| R_D$$

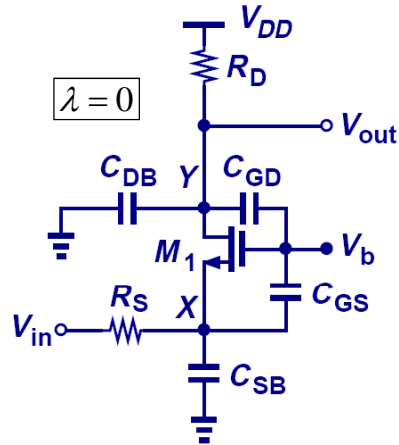EE105 Spring 2008   Lecture 21, Slide 16   Prof. Wu, UC Berkeley

CG Stage: Pole Frequencies

CG stage with MOSFET capacitances shown

$$\omega_{p,X} = \frac{1}{\left(R_S \parallel \dfrac{1}{g_m}\right)C_X}$$

$$C_X = C_{GS} + C_{SB}$$

$$\omega_{p,Y} = \frac{1}{R_D C_Y}$$
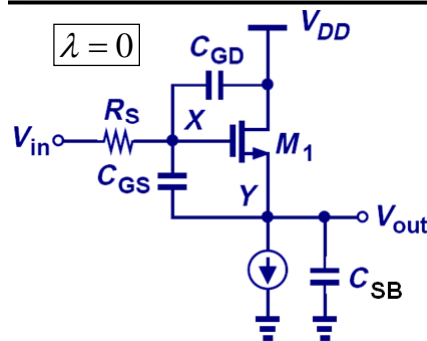
$$C_Y = C_{GD} + C_{DB}$$

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AC Analysis of Source Follower

- The transfer function of a source follower can be obtained by direct AC analysis, similarly as for the emitter follower

$$\frac{v_{out}}{v_{in}} = \frac{1+(j\omega)\dfrac{C_{GS}}{g_m}}{a(j\omega)^2 + b(j\omega)+1}$$

$$a = \frac{R_S}{g_m}\left(C_{GD}C_{GS} + C_{GD}C_{SB} + C_{GS}C_{SB}\right)$$
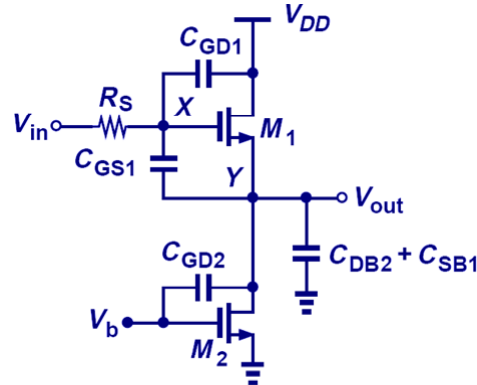
$$b = R_S C_{GD} + \frac{C_{GD}+C_{SB}}{g_m}$$

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Example

$$\frac{v_{out}}{v_{in}} = \frac{1+(j\omega)\dfrac{C_{GS}}{g_m}}{a(j\omega)^2 + b(j\omega)+1}$$

$$a = \frac{R_S}{g_{m1}}\left[C_{GD1}C_{GS1} + (C_{GD1} + C_{GS1})(C_{SB1} + C_{GD2} + C_{DB2})\right]$$

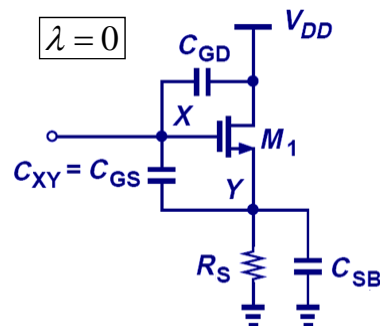$$b = R_S C_{GD1} + \frac{C_{GD1} + C_{SB1} + C_{GD2} + C_{DB2}}{g_{m1}}$$

Source Follower: Input Capacitance

- Recall that the voltage gain of a source follower is $A_v = \dfrac{R_S}{\dfrac{1}{g_m} + R_S}$

Follower stage with MOSFET capacitances shown

- C_{XY} can be decomposed into C_X and C_Y at the input and output nodes, respectively:
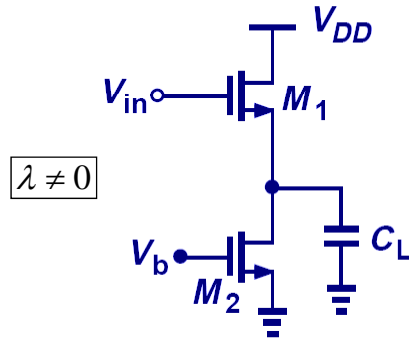
$$C_X = (1-A_v)C_{GS} = \frac{C_{GS}}{1 + g_m R_S}$$

$$C_{in} = C_{GD} + \frac{C_{GS}}{1 + g_m R_S}$$

Example

V_{DD}

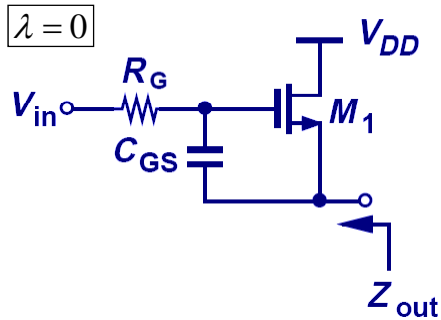V_{in} M_1

$\lambda \neq 0$

V_b M_2

C_L

$$C_{in} = C_{GD1} + \frac{1}{1 + g_{m1}(r_{O1} \| r_{O2})} C_{GS1}$$

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Source Follower: Output Impedance

$\lambda = 0$

R_G

V_{in} M_1 V_{DD}

C_{GS}

Z_{out}

- The output impedance of a source follower can be obtained by direct AC analysis of small-signal model, similarly as for the emitter follower

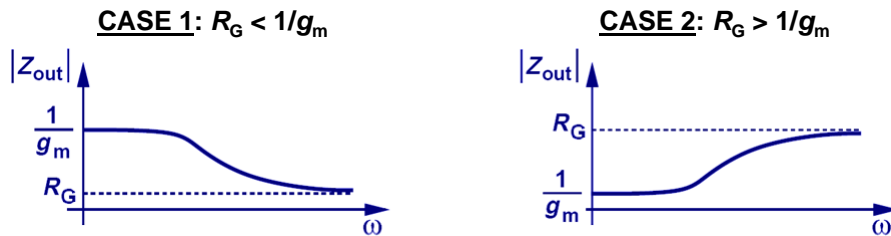$$\frac{v_X}{i_X} = \frac{j\omega R_G C_{GS} + 1}{j\omega C_{GS} + g_m}$$

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Source Follower as Active Inductor

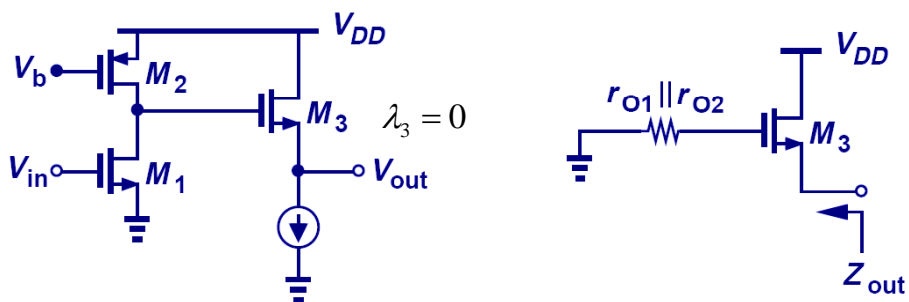$$Z_{out} = \frac{j\omega R_G C_{GS} + 1}{j\omega C_{GS} + g_m}$$

CASE 1: $R_G < 1/g_m$

CASE 2: $R_G > 1/g_m$

- A follower is typically used to lower the driving impedance, *i.e.* R_G is large compared to $1/g_m$, so that the "active inductor" characteristic on the right is usually observed.

Example

$\lambda_3 = 0$

$$Z_{out} = \frac{j\omega(r_{O1} \| r_{O2})C_{GS3} + 1}{j\omega C_{GS3} + g_{m3}}$$

MOS Cascode Stage

- For a cascode stage, Miller multiplication is smaller than in the CS stage.
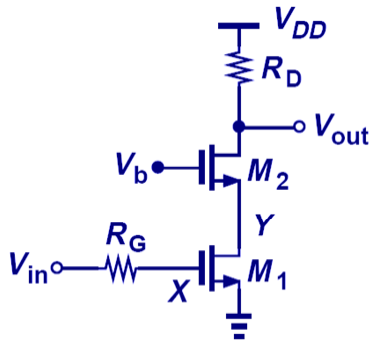
$$A_{v,XY} \equiv \frac{v_X}{v_Y} = -g_{m1}\left(\frac{1}{g_{m2}}\right) \approx -1$$

$$\Rightarrow \quad C_X \approx 2C_{XY}$$
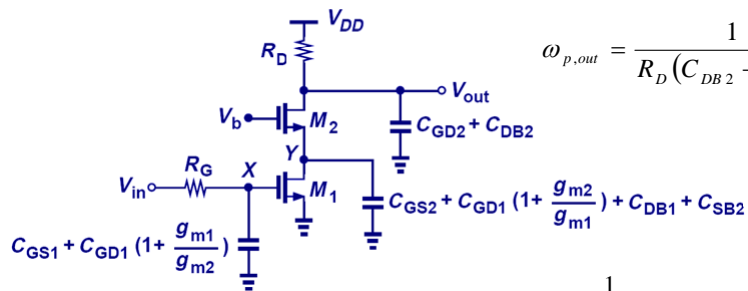
Cascode Stage: Pole Frequencies

$$\lambda = 0$$

Cascode stage with MOSFET capacitances shown
(Miller approximation applied)

$$\omega_{p,out} = \frac{1}{R_D\left(C_{DB2} + C_{GD2}\right)}$$

$C_{GD2} + C_{DB2}$

$C_{GS2} + C_{GD1}\left(1 + \frac{g_{m2}}{g_{m1}}\right) + C_{DB1} + C_{SB2}$

$C_{GS1} + C_{GD1}\left(1 + \frac{g_{m1}}{g_{m2}}\right)$

$$\omega_{p,Y} = \frac{1}{\frac{1}{g_{m2}}\left[C_{DB1} + C_{GS2} + \left(1 + \frac{g_{m2}}{g_{m1}}\right)C_{GD1} + C_{SB2}\right]}$$

$$\omega_{p,X} = \frac{1}{R_G\left[C_{GS1} + \left(1 + \frac{g_{m1}}{g_{m2}}\right)C_{GD1}\right]}$$

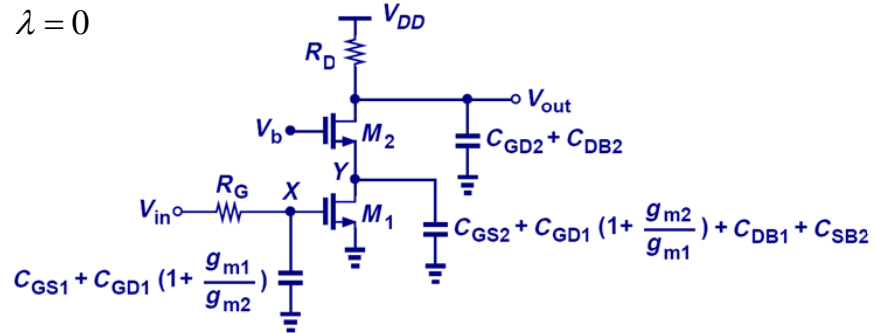# Cascode Stage: I/O Impedances

$\lambda = 0$

$$Z_{in} = \cfrac{1}{j\omega\left[C_{GS1} + \left(1 + \cfrac{g_{m1}}{g_{m2}}\right)C_{GD1}\right]}$$

$$Z_{out} = R_D \,\|\, \cfrac{1}{j\omega(C_{GD2} + C_{DB2})}$$