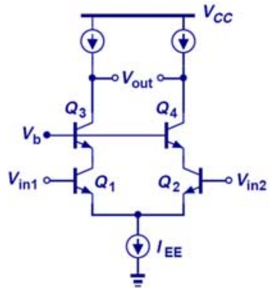
Lecture 23

OUTLINE

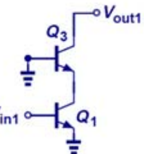
- BJT Differential Amplifiers (cont'd)
  - Cascode differential amplifiers
  - Common-mode rejection
  - Differential pair with active load
- Reading: Chapter 10.4-10.6.1

Cascode Differential Pair



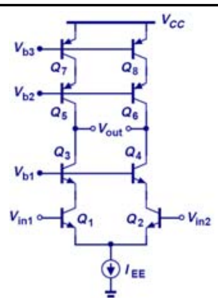
$$R_{out} = [1 + g_{m3}(r_{O1} \| r_{\pi 3})]r_{O3} + r_{O1} \| r_{\pi 3}$$
$$R_{out} \cong g_{m3}(r_{O1} \| r_{\pi 3})r_{O3} + r_{O1} \| r_{\pi 3}$$

Half circuit for ac analysis

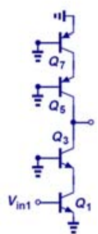


$$A_v = -g_{m1}R_{out} \cong -g_{m1}[g_{m3}(r_{O1} \| r_{\pi 3})r_{O3} + r_{O1} \| r_{\pi 3}]$$

Telescopic Cascode Differential Pair



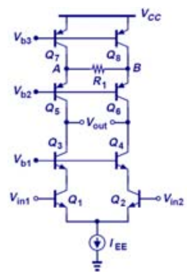
Half circuit for ac analysis



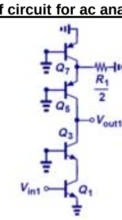
$$A_v \approx -g_{m1}[g_{m3}r_{O3}(r_{O1} \| r_{\pi 3})] \| [g_{m5}r_{O5}(r_{O7} \| r_{\pi 5})]$$

Example

$$R_{op} = \left[1 + g_{m5}\left(r_{O7} \| r_{\pi 5} \| \frac{R_1}{2}\right)\right]r_{O5} + r_{O7} \| r_{\pi 5} \| \frac{R_1}{2}$$
$$A_v = -g_{m1}([g_{m3}r_{O3}(r_{O1} \| r_{\pi 3})] \| R_{op})$$

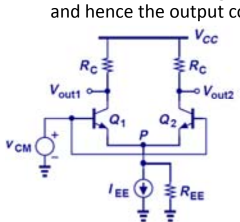


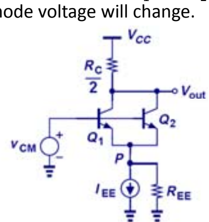
Half circuit for ac analysis



Effect of Finite Tail Impedance

- If the tail current source is not ideal, then when an input common-mode voltage is applied, the currents in Q_1 and Q_2 and hence the output common-mode voltage will change.





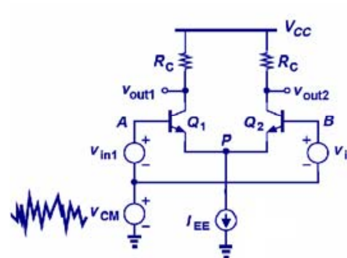
$$\frac{\Delta V_{out,CM}}{\Delta V_{in,CM}} = -\frac{(R_C/2)}{\frac{1}{2g_m} + R_{EE}} = -\frac{R_C}{\frac{1}{g_m} + 2R_{EE}}$$

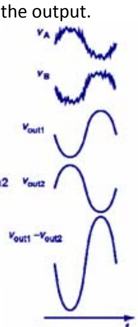
← Common-mode gain should be small

Effect of Input CM Noise

Ideal Tail Current

- There is no effect of the input CM noise at the output.

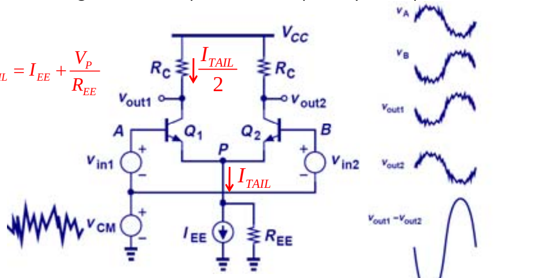




Effect of Input CM Noise
Non-Ideal Tail Current

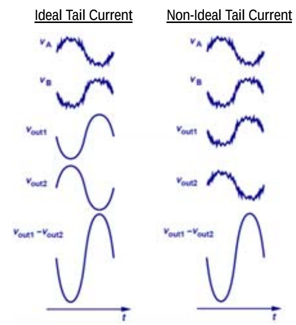
- The single-ended outputs are corrupted by the input CM noise.

$$I_{TAIL} = I_{EE} + \frac{V_P}{R_{EE}}$$



- **Tail current, I_{TAIL}, now changes with V_P, and V_P is affected by V_{CM}**

Comparison



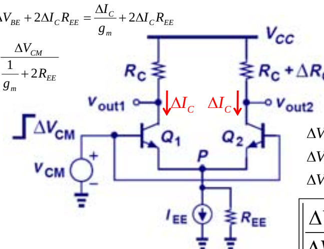
- The *differential* output voltage signal is the same for both cases.
  → **For small input CM noise, the differential pair is not affected.**

CM to DM Conversion; gain A_{CM-DM}

- If finite tail impedance and asymmetry (*e.g.* in load resistance) are *both* present, then the differential output signal *will* contain a portion of the input common-mode signal.

$$\Delta V_{CM} = \Delta V_{BE} + 2\Delta I_C R_{EE} = \frac{\Delta I_C}{g_m} + 2\Delta I_C R_{EE}$$

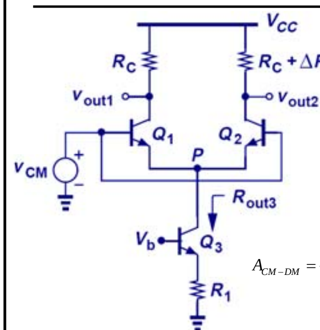
$$\Rightarrow \Delta I_C = \frac{\Delta V_{CM}}{\frac{1}{g_m} + 2R_{EE}}$$



$$\Delta V_{out1} = -\Delta I_C R_C$$
$$\Delta V_{out2} = -\Delta I_C (R_C + \Delta R_C)$$
$$\Delta V_{out} = \Delta V_{out1} - \Delta V_{out2} = -\Delta I_C \Delta R_C$$

$$\left|\frac{\Delta V_{out}}{\Delta V_{CM}}\right| = \frac{\Delta R_C}{(1/g_m) + 2R_{EE}}$$

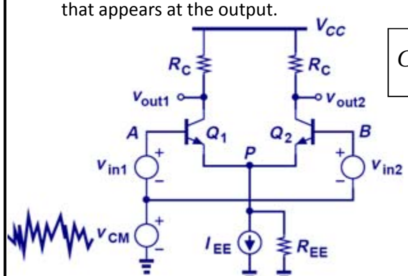
Example



$$A_{CM-DM} = \frac{\Delta R_C}{\frac{1}{g_{m1}} + 2\{[1 + g_{m3}(R_1 \| r_{\pi 3})]r_{O3} + R_1 \| r_{\pi 3}\}}$$

Common-Mode Rejection Ratio

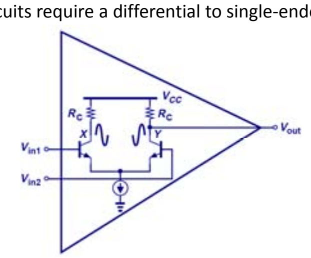
- CMRR is the ratio of the wanted amplified differential input signal to the unwanted converted input common-mode noise that appears at the output.



$$CMRR \equiv \frac{A_{DM}}{A_{CM-DM}}$$

Differential to Single-Ended Conversion

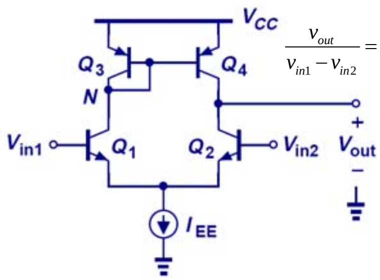
- Many circuits require a differential to single-ended conversion.



- This topology is not very good; its most critical drawback is supply noise corruption, since no common-mode cancellation mechanism exists. Also, we lose half of the voltage signal.

… A Better Alternative

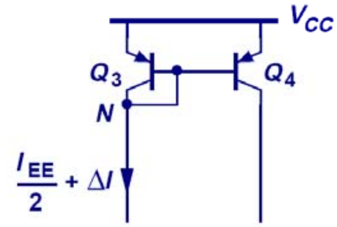
- This circuit topology performs differential to single-ended conversion with no loss of gain.



$$\frac{v_{out}}{v_{in1}-v_{in2}} = g_m\left(r_{o,NPN} \| r_{o,PNP}\right)$$

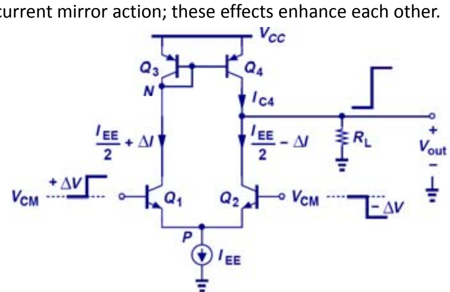
Active Load

- With a current mirror as the load, the signal current produced by Q_1 can be replicated onto Q_4.
- This type of load is different from the conventional "static load" and is called an "active load."



Differential Pair with Active Load

- The input differential pair decreases the current drawn from R_L by ΔI, and the active load pushes an extra ΔI into R_L by current mirror action; these effects enhance each other.



Active Load *vs*. Static Load

- The load in the circuit on the left responds to the input signal and enhances the single-ended output, whereas the load in the circuit on the right does not.