UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 105 — Prof. Pister
Spring 2011

Homework Assignment #11

Due in the 105 box on the 2nd floor of Cory, 5pm Monday 5/2/2011

Problem 1: You have an amplifier with a gain of 1000 and a single pole at 10^7 rad/s. You put it into feedback with a feedback factor of exactly f=0.1.

A. What is the closed-loop pole location?
B. What is the low-frequency closed-loop gain, exactly?
C. If the amplifier gain varies from 1000 to 5000 over process, voltage, and temperature variation, what is the range of the closed-loop gain?
D. What is the low-frequency closed-loop gain error? (Define closed-loop gain error as the % difference between the actual closed-loop gain, and the closed-loop gain if the amplifier were an ideal op-amp with infinite gain).
E. What is the closed-loop gain error at 10^8 rad/sec, 10^9 rad/sec, 10^{10} rad/sec?

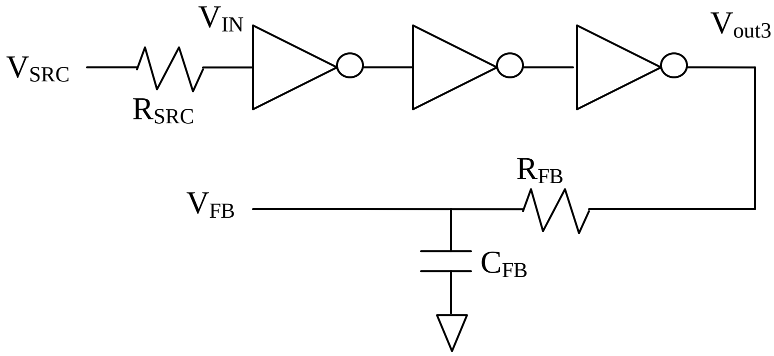
Problem 2: Use spice to simulate your oscillator from the project. Turn in the schematic of your circuit, your spice deck, your hand analysis of the operating point and Bode plot of open loop gain, and your spice simulations of the operating point, Bode plot of open loop gain, and transient analysis showing oscillation. Compare your hand calcs to spice. (note: All of this goes directly into your final project report as well.)

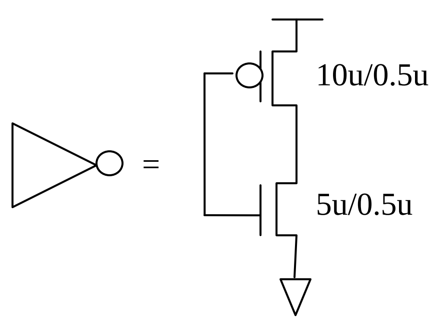
Problem 3: Amplifier or Oscillator?

The circuit below consists of three CMOS inverters, and can be used as an amplifier or an oscillator, depending on the load capacitance. If we make the inverters such that $(W/L)_{PMOS}$ / $(W/L)_{NMOS}$ is the same as the ratio of the N and P mobilities, then the inverters will switch at mid-rail ($V_{DD}/2$). The low-frequency gain through this amplifier is big and negative (180 degrees of phase shift). There are at least 4 poles (can you estimate their magnitude? With t_{ox}=6.9nm, C_{ox}=5fF/um^2). At some frequency those poles will give us another 180 degrees of phase shift, for a total of 360, or 0.

A) Using the spice deck below, plot the open loop gain (magnitude and phase) from V_{IN} to V_{FB}. With C_{FB}=0, what is the unity gain frequency, ω_1? What is the gain when the phase shift around the loop is 360? What is the frequency, ω_{360}? Try the same with C_{FB} set to 50pF, 100pF, and 1nF, and fill in the following table

C_{FB}	ω_1	ω_{360}	$\lvert Af (j\,\omega_{360}) \rvert$
0			
50pF			
100pF			
1nF			





B1) Using spice, connect the feedback node to the input node (IN) with a 0 Ohm resistor. Let V_{SRC} float (spice will give you a warning about node src – that's fine). This circuit is a ring oscillator. With CFB=0, do a transient analysis from 0 to 10ns. What's the period? Does it match what you would expect from part A?
B2) Repeat for C_{FB}=50pF. Simulate from 0 to 1us, and make sure to plot all four nodes: in, out1, out2, out3. Why do we need to simulate for so much longer? Think about what it takes to get the circuit into the high-gain region.
B3) Repeat for C_{FB}= 100pF. What operating point does the circuit settle to after ~0.8us? Smoothly, or with bumps? Zoom in to find the frequency of the bumps.
B4) Repeat for C_{FB}= 1nF. You will need to simulator for ~10us for t his one (why so much longer?).
B5) Fill in the table with your measured period. Do the numbers match? Why does the oscillation not continue with larger capacitors?

C_{FB}	ω_{360} (from part A)	Oscillation frequency
0		
50pF		
100pF		
1nF		

C) Now using the same circuit from part B, with C_{FB}=1nF, and VSRC connected, use spice to generate a closed-loop bode plot of the amplifier. The closed-loop amplifier has a gain of –Rfb/Rsrc, or -1 in this case. What is the pole frequency of the closed-loop amplifier? How does that compare to the pole frequency that you measured in B5? What has feedback done to the pole frequency?
C2) Now plot the transient response of the amplifier to a step input. Does Vout3 faithfully reproduce -1 Vsrc (note that "AC gnd" in this case is the equilibrium point of 1.5V)?

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* HW10, prob. 3: ring oscillator feedback test deck
* having a step in Vdd helps excite oscillations in spice
Vdd dd 0 3 pulse (2.999 3 100p 100p 100p 1m 2m)
.model nmos nmos vto=0.5 tox=6.9nm kp=200u lambda=0.1 capop=0 cgdo=5e-10
.model pmos pmos vto=-0.5 tox=6.9nm kp=100u lambda=0.1 capop=0 cgdo=5e-10
* here's the 3 stage amplifier
m1n out1 in 0 0 nmos w=5u l=0.5u
m1p out1 in dd dd pmos w=10u l=0.5u
m2n out2 out1 0 0 nmos w=5u l=0.5u
m2p out2 out1 dd dd pmos w=10u l=0.5u
m3n out3 out2 0 0 nmos w=5u l=0.5u
m3p out3 out2 dd dd pmos w=10u l=0.5u

* with a feedback resistor to put it in the middle of the high-gain region
Rfb  out3 fb 10k
Cfb  fb 0 1.000n
Rsrc src in 10k

.op
* AC analysis for part A; for part B comment out the Vsrc and .ac lines
* for part C comment out just the Vsrc line
vsrc src 0 1.5 ac 1
.ac dec 10 1k 1000G

* transient analysis for part B; Rfb2 should be commented out for part A
*Rfb2 fb in 0

* transient analysis for part C; comment out for parts A and B
*vsrc src 0 1.5 ac 1 pulse ( 1.4 1.6 1n 1n 1n 100n 200n)

* transient analysis for B and C
*.tran 1p 1000n

.options post
.end
```