UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE105 Lab Experiments

Experiment 2: Diodes, Bipolar Junction Transistors and MOS Characterization

3 Lab

3.1 Diode Parameter Characteristic

Plot $log(I_d) vs. V_d$ curve. Fit the ideality factor of the diode: _____

Plot $I_d vs. V_d$ curve with $100mA$ compliance.

Fit the saturation current I_s: _____, series resistance R_s: _____

Plot $I_d vs. V_d$ curve with $10nA$ upper limit.

Plot $C_D vs. V_R$ curve and $\frac{1}{C_D^2} vs. V_R$.

Extract the zero bias capacitance $C_{jo}A$: _____, built-in voltage V_j: _____.

3.2 Bipolar Junction Transistor Characterization

Plot $I_c vs. V_{CE}$ curves with different I_B.

What is the averaged early voltage V_A: _____

Plot $\beta_F vs. I_C$.

Plot $C_{BC} vs. V$ curve and $\frac{1}{C_{BC}^2} vs. V$.

Extract the zero bias capacitance $C_{jo}A$: _____, built-in voltage V_j: _____.

3.3 MOSFET Characterization

Plot $I_D vs. V_{DS}$ curves with different V_{GS}. Label the cutoff, triode and saturation regions on the plot.

What is the channel length modulation λ: _____.

What is the transconductance G_m with a bias of $V_{GS} = 2.1V$ and $V_{DS} = 1.5V$: _____.

What is the transconductance G_m with a bias of $V_{GS} = 2.1V$ and $V_{DS} = 0.06V$: _____.

Plot $I_D^{\frac{1}{2}} vs. V_G$, extract V_{TH}: _____ and K_n: _____.

Plot $C_{GS} vs. V_{GS}$ curve.

What zero bias drain gate capacitance C_{GD}: _____.