UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE105 Lab Experiments

Lab 5: Multi-Stage Amplifiers

Contents

1 Introduction

Often, a single transistor amplifier cannot satisfy all of the specifications for a given application and an amplifier circuit is designed with multiple cascaded single-transistor amplifiers. In this lab, you will implement a three-stage amplifier, which will amplify an audio signal from a headphone jack and drive a low-impedance speaker.

Make sure to download and print out the Pre-Lab Worksheet and the Lab Worksheet. You may also find the datasheets for the transistors used in this lab to be useful: 2N4401, 2N4403, BS170.

Make sure to complete the Pre-Lab Worksheet before coming to lab. Your lab GSI will check that you have completed the Pre-Lab Worksheet at the beginning of your lab section. Fill out the Pre-Lab and Lab Worksheet while doing the lab and turn them in with supporting traces and plots at the beginning of the first lab section for Lab 6.

2 Pre-Lab

In this prelab, you will be designing an amplifier with the specifications as shown in Table 1. The topology for your design is fixed and is shown in Figure 1.

Don't worry if the circuit in Figure 1 looks daunting. In this prelab, we will go through the design of the circuit step by step.

You will need model files for your NPN BJTs, PNP BJTs, and nMOSFETs to be put into your directory with your `*.sp` file to be able to do HSPICE simulations of your circuit. To include the model files in your `*.sp` file, use the following lines in your `*.sp` file.

Middle Band Gain(A_{mid})	$10 \pm 20\%$
High Cutoff Frequency(f_H)	$\geqslant$ 20kHz
Output Swing(SW)	$\geqslant$ 1 Vpp
Supply Voltage(V_{dd})	5 V
Output load(R_L)	8 Ω

Table 1: Amplifier specification

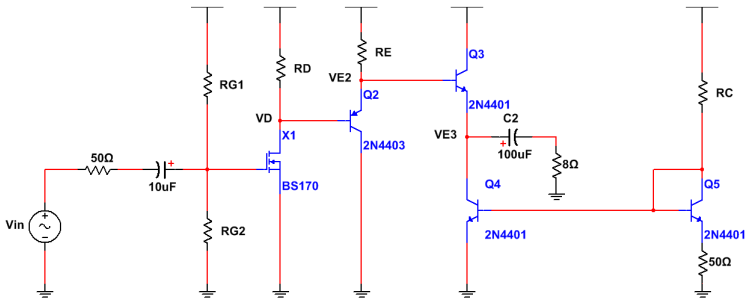

Figure 1: Circuit topology for Lab 5

```
.include npn_2N4401.mod
.include pnp_2N4403.mod
.include mos_BS140.mod
```

To instantiate one of the three types of devices, use the following lines in your `*.sp` file.

```
q<name> <collector> <base> <emitter> BJT_2N4401
q<name> <collector> <base> <emitter> BJT_2N4403
x<name> <drain> <gate> <source> BS170
```

2.1 Back of the envelope determination of DC bias points

On your prelab worksheet, write simple analytical expressions for the DC bias voltages at V_D, V_{E2}, V_{E3}. You may leave your expressions in terms of V_{be}, I_D, etc. Ignore base currents and assume that the bipolar transistors have an infinite Early voltage and that the MOSFET has no channel-length modulation.

2.2 Input stage

The purpose of the input stage is to present a high input impedance to the voltage source and to provide voltage gain for the amplifier. Shown below in Figure 2 is the input stage of the amplifier.

Since you are now an expert at designing common-source amplifier circuits after having completed Lab 3, design the first stage to have a gain of $10 \pm 20\%$. Make sure that the drain voltage bias point will be compatible with the bias points required for the later stages and that the output voltage swing is greater than 1 Volt. Use the nMOS device parameters that you characterized in Lab 2 for this stage. First do a back-of-the envelope hand calculation for your design, and verify your design and tweak parameters to achieve the specifications in HSPICE.

In your prelab worksheet, write down the midband (no capacitors) small signal circuit for the input stage. Also write expressions for the midband gain, output resistance, and output swing. Fill out the tables in your prelab worksheet with the numerical values you obtained from hand calculation and simulation. In HSPICE, you can calculate the small signal output resistance by using the following command and by looking in the HSPICE output file `*.lis`.

```
.tf v(<drain>) <input voltage source name>
```

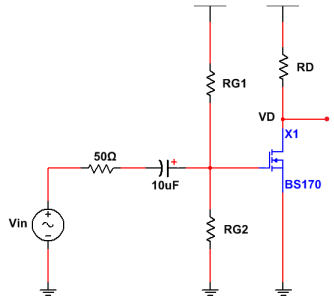

Figure 2: First stage circuit topology

2.3 Output stage

Next, we will jump ahead and design the output stage. The purpose of the output stage is to provide enough current to be able to drive the low impedance 8 Ω speaker load. We will first analyze and design the common collector circuit with current source bias, and then later design an implementation of the current source. Again, design is to be done using hand calculations, followed by verification and design tweaking in HSPICE.

2.3.1 Determination of bias current

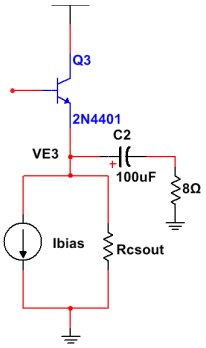

Figure 3: Output stage circuit topology, current source circuit not shown

The only design parameter for this stage is the current source value I_{bias}.We will do both a small signal and large signal analysis of the output stage and figure out two constraints for the value of the current source.

In your prelab worksheet, write down the small signal midband circuit for the output stage with 8 Ω speaker load, and write expressions for the the midband voltage gain and and input resistance of the circuit. How much bias current do we need to be able to get a voltage midband gain of 0.9? 0.99? Let $R_{csout} = r_o$ of the 2N4401 NPN transistor.

Next, analyze the output swing of the output stage, referring to the diagram in Figure 4. Treat the capacitor as an AC short. What is the maximum ac current that can be sourced from the supply? What is the maximum ac current that can be sunk to ground? What are the maximum and minimum output voltages of the stage, defining the output swing? Write expressions for the four values in your prelab worksheet.

From the expression for the minimum output voltage, what bias current is required to achieve a 1 Vpp or 0.5 V amplitude output swing? Write this value in your worksheet, and use this value in your design. Check the datasheet for the 2N4401 NPN transistor, and make sure that your designed I_{bias} is not higher than the maximum collector current rating, and that the power dissipation $P = I_{bias} \times V_{ce}$ in the bipolar transistor Q3 is less than the maximum power rating.

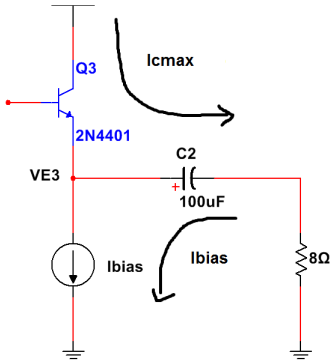

Figure 4: Output swing analysis showing maximum current excursions. For simplicity, the output resistance of the current source is not shown.

2.3.2 Current source design

Shown in Figure 5 is a diagram showing the current source circuit. The current source circuit is comprised of two parts. The right branch is a circuit which generates a bias voltage for the base of npn bipolar transistor Q4 on the left branch, which is acting as a current source load. Here, the design is to choose the proper value of R_C to generate the desired I_{bias}.

If you need help with the design, try the following method. Ignoring V_{ce} dependence on I_C and using KVL on the loop indicated on Figure 5, write an expression relating I_{bias} and I_{source}, and numerically solve for I_{source}. Next, applying KCL to the node connected to the two bases of the transistors, write an expression relating R_C to I_{bias} and I_{source}, and numerically solve for R_C.

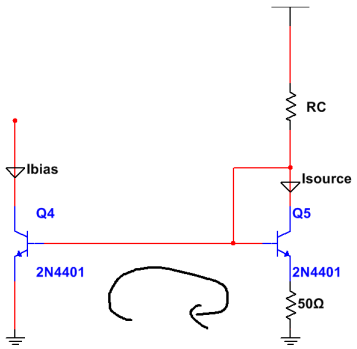

Figure 5: Current source circuit

Fill out the tables in your prelab worksheet with the numerical values you obtained from hand calculation and simulation. For the small signal values, **make sure to do the HSPICE simulations of the full output stage with transistor current source circuit and speaker load, and to set a DC bias voltage equal to V_{E2} for the input of transistor Q3!** The hand calculation small signal values can be the values you calculated for the circuit with the transistor load modelled as a current source. In HSPICE, you can calculate the small signal input resistance by using the following command and by looking in the HSPICE output file `*.lis`. Attach to your prelab worksheet a plot showing the full output swing of the output stage.

```
.tf v(<emitter of Q3>) <input voltage source name>
```

2.4 Middle stage

The middle stage primarily serves as an AC and DC buffer between the two stages. If we were to directly cascade the input and output stages together, the following two things would happen:

1. Because the bias current of the output stage is so much higher than the input stage, the base of the output drive transistor Q3 would draw significant current from R_D and and totally alter the output bias point of the input stage.

2. The output impedance of the input stage and the input impedance of the output stage are of similar magnitudes. Not all of the voltage generated by the input stage would be coupled to the output stage due to the loading effect.

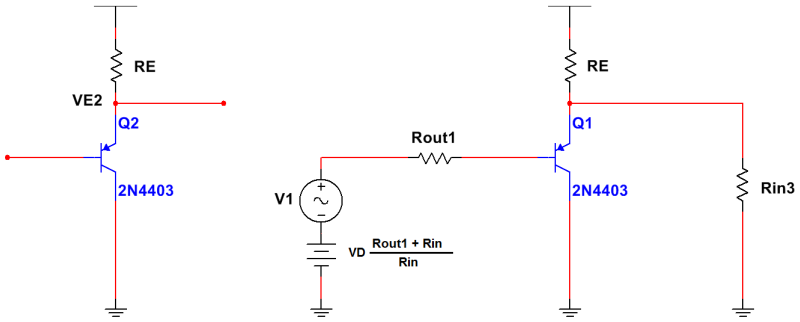

Figure 6: Middle stage circuit without and with input and output loading

Shown in Figure 6 is the common collector circuit topology for the middle stage. The common collector topology is a good choice here because its output voltage bias point is not very sensitive to the bias current and because the common collector circuit has a high input impedance and a low output impedance, which is exactly what we need to couple voltage generated by the input stage to the output stage.

For this stage, the only design parameter is R_E. The following exercises will guide your design decision for the value of R_E. **With loading from the output resistance of the input stage and input resistance of the output stage**, draw the small signal circuit and write an expression for the 'loaded gain' of the circuit shown in Figure 6. It is important to notice that V_{E2} is mostly independent of R_E, and so the value of R_E sets the bias current as well as appears in the small signal circuit.

Next, we analyze the output swing of V_{E2}. What are the maximum and minimum output voltages of the stage, defining the output swing? Write expressions for these values in your prelab worksheet. Choose a value for R_E that both provides a loaded gain close to 1 and allows for a swing greater than 1 Vpp. Fill out the tables in your worksheet with the numerical values you obtained from hand calculation and simulation of the middle stage.

2.5 Putting it all together

Now that you have designed and verified each of the three stages, cascade them together as shown in Figure 1. Simulate in HSPICE the frequency response from 1 Hz to 20 kHz and verify the output swing of the entire circuit. Attach plots of the frequency response as well as a plot showing evidence of a 1 Vpp output swing of the entire amplifier.

3 Lab

Please don't forget to set a current limit on your power supply! 150 mA is a reasonable value to set for the current limit. The components that you will need in Lab 5 are listed in Table 2.

Component	Quantity
BS170(NMOS)	1 (the one you already characterized)
2N4403(PNP)	1 (no need to characterize)
2N4401(NPN)	3 (no need to characterize)
100 uF capacitor	1
8 Ω speaker	1
10 uF capacitor	1
100 kΩ pot	1
10 kΩ pot	1
1 kΩ pot	1
Resistors	Various Values

Table 2: Lab 5 components

3.1 First stage

While you are not obligated to build the input stage exactly as shown in Figure 7, with the two potentiometers, the author thinks that it is a good idea to do so. Adjusting the two potentiometers gives you two almost totally independent knobs to tune I_d and R_D to achieve your desired gain and drain voltage bias.

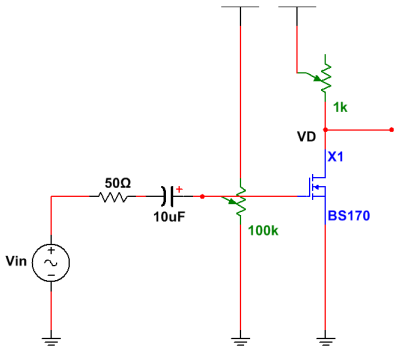

Figure 7: Input stage circuit

Measure the gain, DC output voltage, and output swing of this circuit, and write these values in your lab worksheet. Also write the component values of your designed circuit in your worksheet.

Also measure the output resistance of the circuit by loading the drain of the circuit shown in Figure 7 with a shunt resistor to ground approximately equal to the output resistance that you calculated in the prelab. The output AC voltage amplitude should drop by about one half. Calculate the output resistance from the AC output voltage measurement of the loaded circuit.

You may want to place a 100 uF capacitor in series with the loading resistor to prevent DC current from flowing into the loading resistor and altering your drain voltage bias point, if you think that that will alter the output resistance measurement by a lot. If you decide to do this, make sure that you measure the AC output voltage at a frequency where the coupling capacitor looks like a short circuit. Ask your lab GSI if you are confused by this discussion regarding output resistance measurement.

Make sure to capture a single oscilloscope trace with both input voltage and output voltage waveforms demonstrating the circuit's gain, output voltage, and swing and include it with your lab worksheet. This

means that in addition to measuring the AC amplitudes of the input and output waveforms, you must also measure the DC offset of the output waveform. Ask your lab GSI if you do not know how to do this. Also capture an oscilloscope trace with both input and output voltage waveforms showing the output resistance measurement.

3.2 Output stage

Build the circuit shown in Figure 8. Since we are pushing the transistors sort of close to their power dissipation limits, they will heat up, and so their I-V characteristics will drift a little bit. Because no special effort was taken by the author to ensure that the circuit design of the output stage has perfect temperature stability, the bias current will drift a little bit as the transistors heat up. You may need to adjust the 10 kΩ potentiometer a little bit to compensate for the bias current fluctuating as the transistors heat up.

If we have enough transistors in the lab, you can try putting 2x 2N4401 transistors in parallel in place of Q3 and Q4 to halve the power dissipation in each device. You may have to readjust R_C to ensure that the correct I_{bias} is flowing through both transistors. This may help with the temperature stability somewhat.

Since the input at the base of Q3 is not being biased by virtue of being connected to the rest of the three stage circuit, you will need to add a DC bias to the input for the circuit manuallly. You can decide to design a resistor bias network with coupling capacitor to DC bias the base and to couple in the AC input voltage, but honestly, it is easier to directly connect the function generator to the base and add a DC offset to the AC voltage. **If you are using the function generator in its default 50 Ω output impedance mode, make sure to remember that both the AC and DC voltage generated by the function generator are a factor of 2 greater than what is displayed on the front panel!** Also remember to account for the 50 Ω output impedance of the function generator, if you think that it will matter.

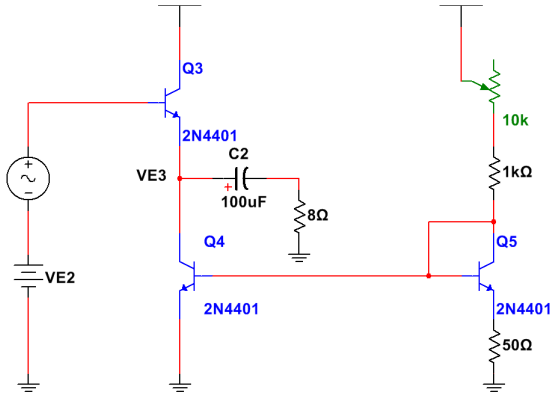

Figure 8: Output stage circuit

Measure the gain and output swing of the stage, and write these values in the table in your lab worksheet. Also write the component values of your designed circuit in your worksheet.

Also measure the input resistance of the circuit shown in Figure 8 by placing a resistor in series with the function generator and the output stage with a magnitude equal to the input resistance of the stage that you calculated in the prelab. The amplitude of the AC voltage at the output of the stage should be approximately halved. Infer the input resistance from this reduced amplitude of the AC output voltage.

Make sure to increase the input bias voltage so that the base of Q3 is biased to V_{E2}! About one half of the input DC voltage will be dropped across the resistor that you added to the circuit. It is probably smart to measure the DC offset of the base of Q3 on the oscilloscope so you know how much DC voltage to set in the function generator. Ask your lab GSI if you are confused by this procedure for input resistance measurement.

Make sure to capture a single oscilloscope trace with both input voltage and output voltage waveforms demonstrating the circuit's gain and swing and add it to your worksheet. Also capture an oscilloscope trace with both input and output voltage waveforms showing the input resistance measurement.

3.3 Middle stage

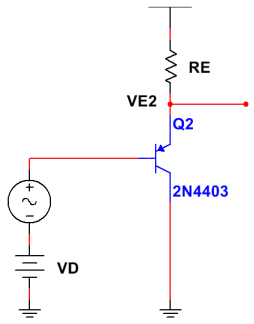

Figure 9: Middle stage circuit

Measure the **unloaded** gain and swing of the stage. You will have to bias the input just like in the measurements of the output stage. Also measure the input and output resistance in the same manner as the measurements of the previous stages. Write these values in your lab worksheet.

Capture an oscilloscope trace demonstrating gain and swing and include it with your lab worksheet. Also capture oscilloscope traces for the input and output impedance measurements and attach them to your lab worksheet.

3.4 Putting it all together

Cascade the three stages together as shown in Figure 1 and measure the DC voltages at V_D, V_{E2}, and V_{E3}. Write the values in your lab worksheet. Measure the gain and output swing of the circuit and write the values in your worksheet. Capture an oscilloscope trace demonstrating that the entire circuit meets the gain and swing specifications. For fun, you can ask your GSI to plug your circuit into the computer and play audio. The author recommends the following educational YouTube video: https://www.youtube.com/watch?v=PWYM8D8ABFM.