**UNIVERSITY OF CALIFORNIA AT BERKELEY**
**College of Engineering**
**Department of Electrical Engineering and Computer Sciences**

**EE105 Lab Experiments**

# Lab 6: Differential Amplifier Prelab

## Contents



## 1 Introduction

In certain applications, you only want to amplify the difference (which carries the useful information) of the two input signals but suppress the common part (most likely the noise) of them. Differential amplifier satisfies such requirement with its superior high differential signal gain over the common signal input. In this lab, you will design and test a simple resistor loaded differential amplifier with current mirror bias.

## 2 Design Specs

The overall schematic is shown in Figure 1. Q1 and Q2, Q3 and Q4 are matched transistor pairs. R1 and R2 are matched resistor load. Q1 and Q2 form the differential input stage; Q3 and Q4, along with R3 and R4, function as a Widlar current source that biases differential pair. C1 and C2 are bypass capacitors, $C_l$ is the output load capacitor; $V_{cm}$ is the common input signal, $V_{dm}$ is the differential input signal. The design specs for the differential amplifier is shown in the table below.

**Table 1:** Design Specification

| | |
|---|---|
| Differential Signal Gain $((V_{o1} - V_{o2})/V_{dm})$ | $\geqslant 80$ |
| Differential Signal High Cutoff Frequency $(f_{H_{dm}})$ | $\geqslant$ 20kHz |
| Differential Output Swing $(V_{o1} - V_{o2})$ | $\geqslant$ 2V (peak to peak) |
| Supply Voltage $(V_{DD}/V_{SS})$ | 10V/-10V |

## 3 Differential Input Stage

The simplified differential input stage is shown in Figure 2. Q1 and Q2 is the matched transistor pair. R1 and R2 are the matched resistors. We first simplify the Widlar current source as an ideal current source in parallel with its output impedance. Please draw the equivalent "half-circuit" for differential signal and derive the differential signal gain($A_{dm} = (V_{o1} - V_{o2})/V_{dm}$). In this way, you simplify the design of a differential

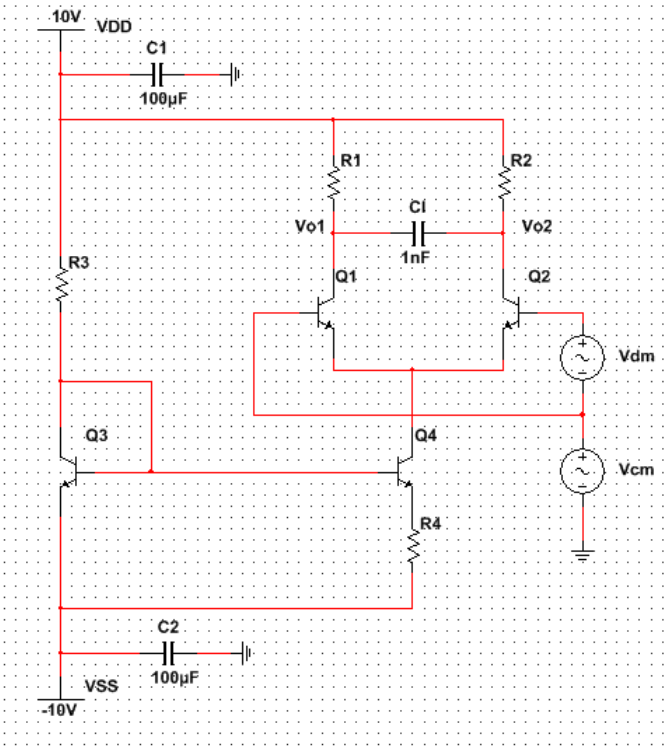


**Figure 1:** Overall Schematic

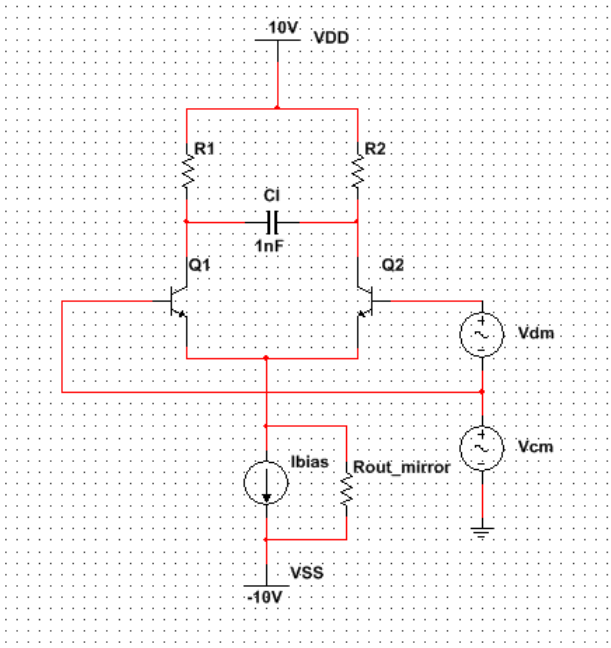


**Figure 2:** Simplified Differential Input Stage

amplifier into a single transistor amplifier. The only design parameter here is the tail current source , R1 and R2. According to the gain and bandwidth requirement, determine the R1 and R2 as well as $I_{bias}$. Right now you can assume the base voltage of Q1 and Q2 are biased correctly. Later on, we will check operation range of the base voltage of the differential pair.

# 4 Widlar Current Source

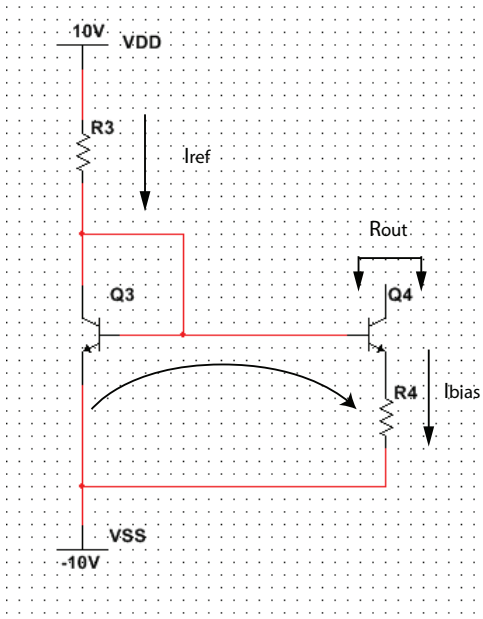


**Figure 3:** Widlar Current Mirror

From the previous section, you already know the value of the tail current source you need to achieve the desired gain and bandwidth. In this section, we will go ahead and design such a current source.

The standard Widlar current mirror is redrawn in Figure 3. Q3 and Q4 are a matched transistor pair, you need to select proper resistor value for R3 and R4 to generate the desired $I_{bias}$.

For hand calculation, to start with, please write down the expression with the KVL on the loop as indicated in Figure 3 and arrange the equation so that only $I_{ref}$, $I_{bias}$, R4 and the thermal voltage $V_t$ remain.(Hint: $V_{be3} - V_{be4} = V_t \cdot ln(\frac{I_{C3}}{I_{C4}})$ and you can assume $\alpha = 1$) Select proper $I_{ref}$ and R4 so that $I_{bias}$ equals the design value.

Then write down the equation relating $I_{ref}$, $V_{be3}$, R3 and supply voltages. By assuming $V_{be3} = 0.7$, you could determine the resistance of R3.

After getting the R3 and R4, you can derive the output impedance of the current source from the small signal model. What's the minimal allowable voltage on the collector of the transistor Q4 to ensure the current source work properly?

Use the Hspice simulation to verify the characteristics of current source. In the simulation, you can connect the the collector of Q4 through a resistor to VDD and make sure the the collector voltage of Q4 is above 0. You can tune R3 so that $I_{bias}$ is exactly what you need but the most important thing is to get a taste of how $I_{bias}$ changes with R3 and R4.

# 5 Common Mode Characterization

With the characteristics of the current source. Let's go back to Figure 2 and check the common mode performance. Now please draw the equivalent "half-circuit" for the common mode signal. Draw the

small signal model of the common mode half circuit. Now assume you have 0.1% resistor mismatch (R1=99.9%R2), please calculate the common-mode gain($A_{cm} = (V_{o1} - V_{o2})/V_{cm}$) and the common-mode rejection ratio($CMRR = A_{dm}/A_{cm}$).

What's the minimal common mode input voltage? (Hint: minimal common mode input voltage makes sure Q4 is always in active region) What's the maximum common mode input voltage? (Hint: maximum common mode input voltage makes sure Q1 and Q2 are always in active region)

# 6 Put it together

Now connect the current mirror with the differential input stage. Verify all the design specs in the Hspice simulation and tune the design parameter if necessary.