University of California, Berkeley *Fall 2016*
EE 105 *Prof. A. M. Niknejad*

Final Exam (closed book/notes)

Last Name	First Name
SID	
EE 20/40 or 16AB	

Guidelines: Closed book. You may use a calculator.
Do not unstaple the exam. In order to maximize your score, write clearly and indicate each step of your calculations. We cannot give you partial credit if we do not understand your reasoning. Feel free to use scratch paper but copy the final results to the exam (do not staple any additional sheets).

The resistance of a material is related to the physical dimensions and resistivity by

$$R = \frac{\rho L}{tW} = \frac{\rho}{t}\frac{L}{W} = R_{sq}\frac{L}{W}$$

The capacitance of a parallel plate structre is given by

$$C = \frac{\epsilon A}{d}$$

The conductivity of a material depends on charge density (n and p), mobility $\mu_{n,p}$, and charge of carriers q_e:

$$\sigma = q_e(\mu_n n + \mu_p p)$$

Note that mobility is defined through the drift velocity, $v = \mu E$ where E is the electric field. An instrinsic semiconductor has a doping concentration of $n_i = p_i = 1.4 \times 10^{10}\text{cm}^{-3}$. A pn junction has a built-in potential given by

$$\phi_{bi} = \frac{kT}{q}\ln\frac{N_a N_d}{n_i^2}$$

and a depletion region width of (for a reverse bias voltage of V_{rev})

$$W_{dep} = \sqrt{\frac{2\epsilon_s(\phi_{bi} + |V_{rev}|)}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)}$$

where the permittivity of Si is given by

$$\epsilon_s = 11.9 \times 8.854 \times 10^{-14} \frac{\text{F}}{\text{cm}}$$

The thermal voltage at room temperature T is given by

$$V_t = \frac{kT}{q} \approx 26\text{mV}$$

where $q = 1.6 \times 10^{-19}$C is the charge of an electron.
MOS Square Law Device Physics (Saturation)

$$I_{DS} = \mu C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$C_{gs} = \frac{2}{3} W \cdot L C_{ox}$$

$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}} \approx \frac{3}{2} \frac{\mu (V_{GS} - V_T)}{L^2}$$

The transconductance is given by

$$g_m = \frac{dI_{ds}}{dV_{gs}} = \mu C_{ox} \frac{W}{L} (V_{gs} - V_t) = \frac{2 I_{DS}}{V_{gs} - V_t} = \sqrt{2 \mu C_{ox} \frac{W}{L} I_{ds}}$$

In the triode region, we have

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) (1 + \lambda V_{DS})$$

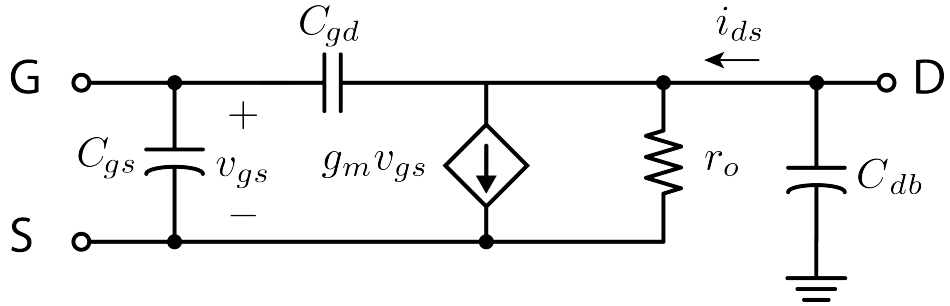
$$C_{gs} = C_{gd} = \frac{1}{2} W \cdot L C_{ox}$$

Miller's Theorem allows us to replace an impedance Z between two nodes with two impedances to ground at node 1 and 2:

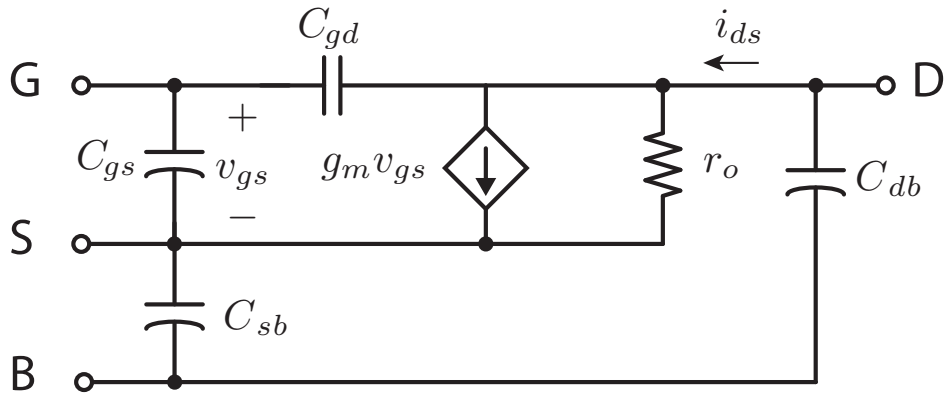
$$Z_1' = \frac{Z}{1 - A_0}$$

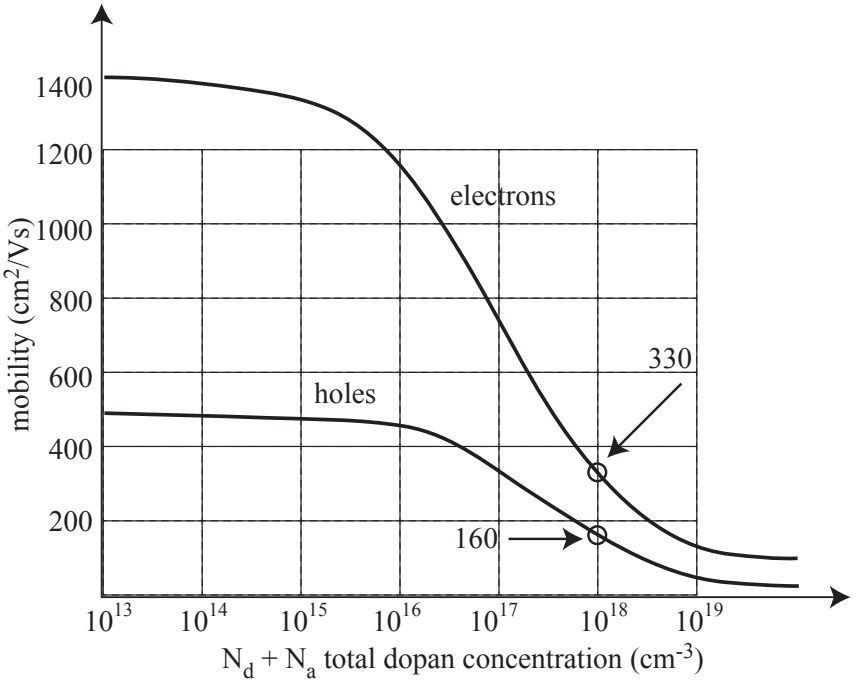
$$Z_2' = \frac{Z}{1 - A_0^{-1}}$$

where $A_0 = v_2 / v_1$ is the voltage gain between the nodes.
A 3-termianl transistor can be represented by its small-signal equivalent circuit shown below:

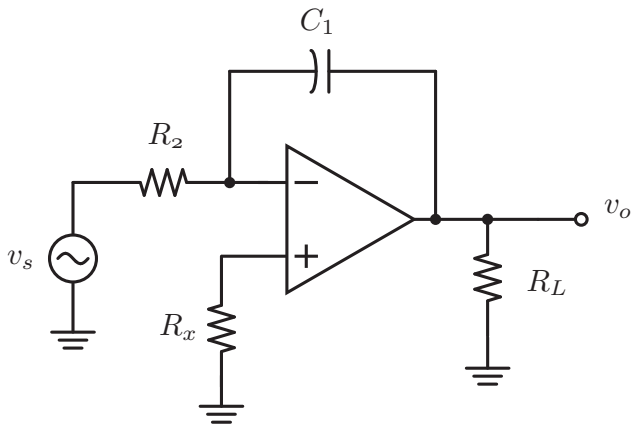


A 4-termianl transistor can be represented by its small-signal equivalent circuit shown below:





1. (20 points) An op-amp is configured as shown below.



(a) (4 points) Assuming the op-amp is ideal, find the transfer function to the output.

(b) (4 points) What are the poles and zeros of the transfer function?

(c) (4 points) Suppose the input is a step function that transitions from 0V to 1V at a time $t = 0$s. Plot the output voltage and carefully label the time scale. Assume the op-amp has a slew-rate of $1\text{V}/\mu\text{s}$. Use the following values: $C_1 = 100\text{pF}$, $R_2 = 1\text{k}\Omega$, $R_L = 100\Omega$, $R_x = 1\text{M}\Omega$.

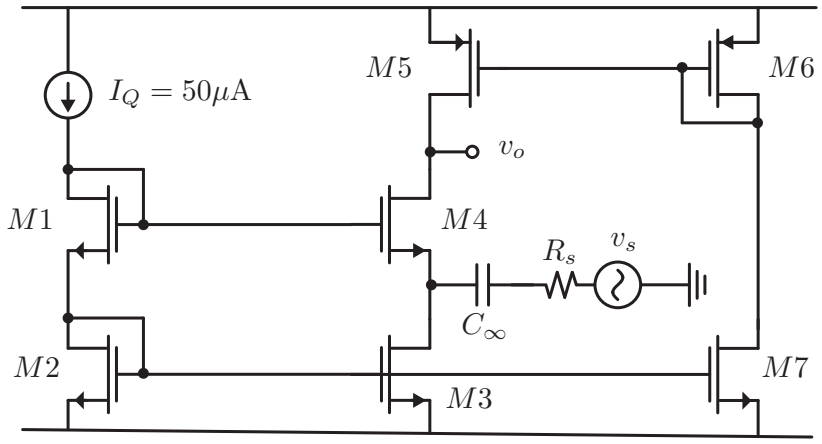
(d) (4 points) Now suppose that the op-amp has infinite DC gain but has a unity gain frequency ω_u:

$$A(\omega) = \frac{\omega_u}{j\omega}$$

Re-derive the transfer function and state the poles and zeros explicitly.

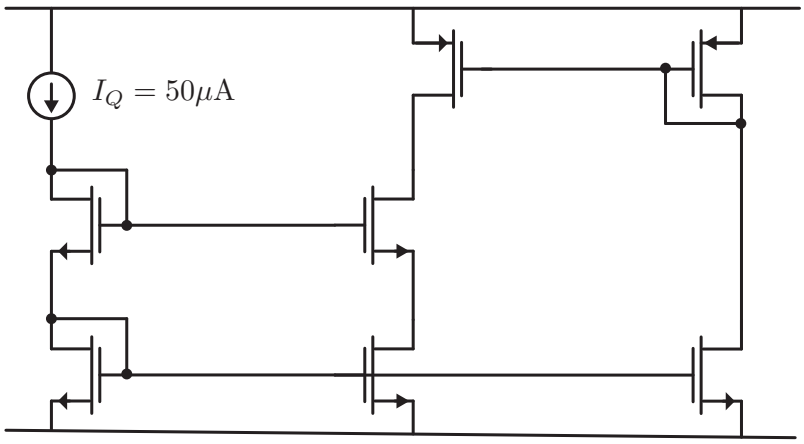
(e) (4 points) The op-amp has an input bias current of 1nA that flows into both input terminals and operates on power supply rails of ± 5V. Calculate the output DC offset voltage. Suggest a nulling strategy.

2. (20 points) An amplifier is shown below. Both PMOS and NMOS transistor have $\mu C_{ox} = 100\mu\text{A/V}^2$, a threshold voltage of $\pm 0.5\text{V}$. You may assume square law behavior. Device dimensions are as follows: $(W/L)_1 = (W/L)_2 = 1$, $(W/L)_3 = (W/L)_4 = (W/L)_5 = 5$, $(W/L)_6 = (W/L)_7 = 10$. Assume $\lambda = 0.05\text{V}^{-1}$. Suppose that $V_{DD} = 5\text{V}$ and $V_{SS} = 0\text{V}$. The source resistance $R_s = 4\text{k}\Omega$.



We will ignore the device parasitic capacitances for parts (a)-(d).

(a) (4 points) Find all DC currents and DC voltages in the circuit and label them below. Make approximations and neglect λ in your calculations unless absolutely necessary.



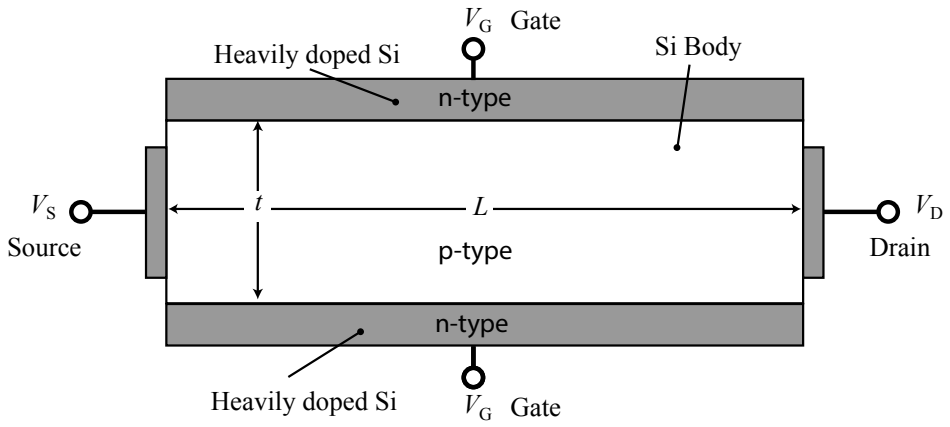
(b) (4 points) Identify the signal path and redraw the circuit and the relevant components. Do not draw a small-signal model. If you ignore a device, include the equivalent circuit for it.

(c) (4 points) Draw the small-signal circuit. You may neglect devcies that are not important for calculation of voltage gain.

(d) (4 points) What is the voltage gain? You may make approximations here.

(e) (4 points) What is the approximate 3-dB bandwidth of the circuit? Assume $C_{gs} = 0.2\text{pF}$ and $C_{gd} = 0.05\text{pF}$ for all transistors.

3. (30 points) A device known as a Junction FET (JFET) is shown below. It is built from a conducting piece of semiconductor (p-type) sandwiched between two heavily doped gate regions (n-type) that act like ideal conductors (shorted to each other) and the source/drain are modeled as perfect conductors at either end for simplicity. Ignore end-effects (assume 1D profiles). The device length $L = 1\mu$m, $W = 100\mu$m (into the page) and the thickness $t = 10\mu$m. Assume the gate has a doping of 10^{20}cm^{-3}.



(a) (3 points) If the semiconductor is intrinsic Si (and not p-type as labled), what is the resistance of the structure? Ignore the gates and their influence on the structure for this problem. Just assume it's a silicon slab of given dimensions. This is a "warm up" problem.

(b) (3 points) To dope the body p-type as shown, should we add a group 3 or group 5 element? Explain. After doping, what is the free hole concentration ? Explain.

(c) (3 points) If the semiconductor is now doped with a concentration of 10^{18}cm^{-3}, what is the resulting resistance of the rectangular cross section shown? Ignore the gates and their influence on the structure for this problem. Just assume it's a doped silicon slab of given dimensions. Use the provided graph in the "cheat sheet".

(d) (3 points) Now suppose that the gate voltages are biased with a positive voltage. What do you expect to happen? Draw a picture and explain your figure. Assume both the drain and source are grounded.

(e) (5 points) For a gate bias of 0.5V, what is the drain-source current when a V_{DS} is applied?

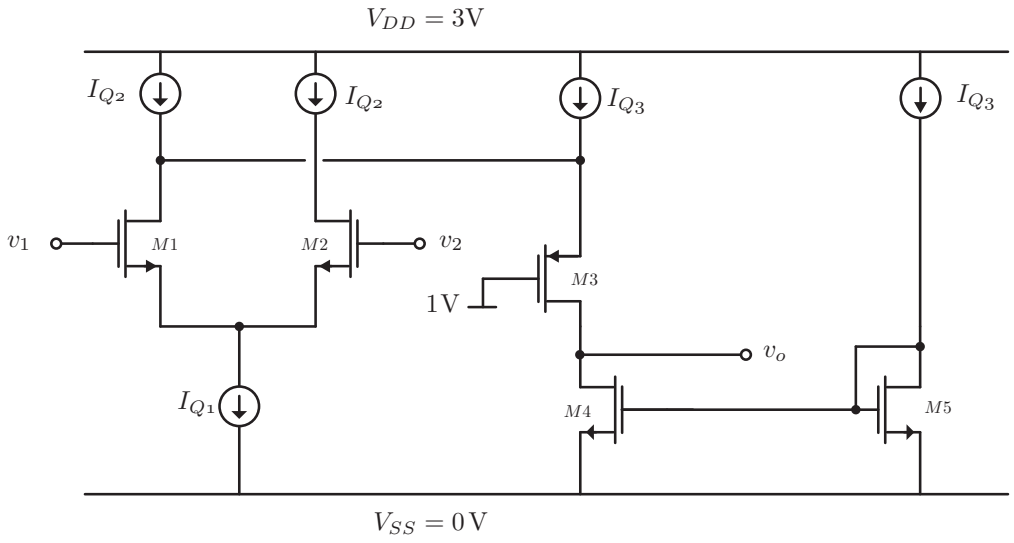
(f) (3 points) Can you explain how this structure acts like a transistor? Does the current increase or decrease with increasing gate bias? Explain how the gate controls the channel.

(g) (4 points) Can you explain why the device current will eventually saturate if we bias the drain voltage to some high negative value? What is happening in the device?

(h) (3 points) Show the physical origin of the capacitors in this structure.

(i) (3 points) Derive the complete small-signal model and draw a small-signal model. You should do it symbolically, there is no need to carry out the calculations.

4. (30 points) A differential amplifier is shown below. $I_{Q1} = 200\mu$A, $I_{Q2} = 150\mu$A, and $I_{Q3} = 50\mu$A. Assume transistors are biased with $V_{dsat} = .4$V and $\lambda = .025\text{V}^{-1}$. The device $|V_T| = 0.25$V. Current sources are ideal.



(a) (2 points) Please identify the input v^+ and v^-, labeled as v_1 and v_2.

(b) (7 points) Find the DC voltages and currents in the circuit when the inputs are at DC 1.5V. Approximations are highly encouraged, especially neglecting output resistance (λ) unless absolutely necessary.

(c) (7 points) What is the DC gain of the amplifier for a differential input.

(d) (7 points) If the amplifier drives a load of 1MΩ (AC coupled), how does the gain change?