HW#6
### (Submit to bCourses by 11 pm on 3/15)

1) Calculate the total charge stored in the channel of an NMOS transistor having $C_{ox} = 9\ fF/\mu m^2$, $L = 0.36\ \mu m$, and $W = 3.6\ \mu m$, and operated at $V_{OV} = 0.2$ V and $V_{DS} = 0$ V.

2) Consider a CMOS process for which $L_{min} = 0.36\ \mu m$, $t_{ox} = 6\ nm$, $\mu_n = 460\ cm^2/V \cdot s$, and $V_t = 5$ V.
   a) Find C_{ox} and k'_n.
   b) For an NMOS transistor with W/L = 20 μm/0.25 μm, calculate the values of V_{OV}, V_{GS}, and $V_{DS,min}$ needed to operate the transistor in the saturation region with a dc current $I_D = 0.5$ mA.
   c) For the device in (b), find the values of $V_{OV\ and}$ V_{GS} required to cause the device to operate as a 100 Ω resistor for very small v_{DS}?

3) The NMOS transistor in the circuit below has $V_t = 0.4$V and $k_n = k'_n(W/L) = 4\ mA/V^2$. The voltages at the source and the drain are measured and found to be -0.6 V and + 0.2 V, respectively. What currents I_D is flowing, and what must the values of R_D and R_S be? What is the largest value for R_D for which I_D remains unchanged from the value found?
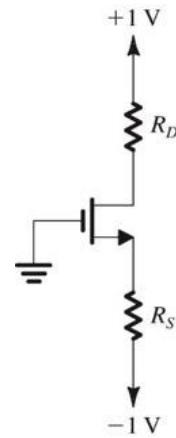
4) The NMOS transistor in the circuit below has $V_t = 0.5$ V, $k'_n = 0.25\ mA/V^2$, $\lambda = 0$, and $L_1 = L_2 = 0.25\ \mu m$. Find the required values of the gate width for Q_1 and Q_2, and the value of R, to obtain the voltage and current values indicated.