UC Berkeley **EE105** **Spring 2019**

HW#8

(Submit to bCourses by 11:59 pm on 4/21, Sunday)

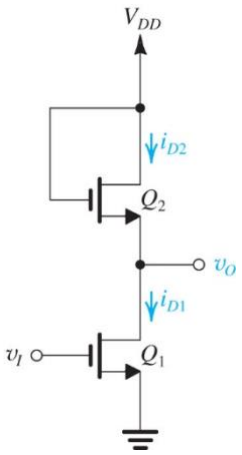
1) The circuit shown on the right is a common source amplifier with a diode-connected NMOS load, Q_2. Using $i_{D1} = i_{D2}$, show that for the range of v_I over which Q_1 is operating in saturation, that is, for

$$V_{t1} \le v_I \le v_o + V_{t1}$$

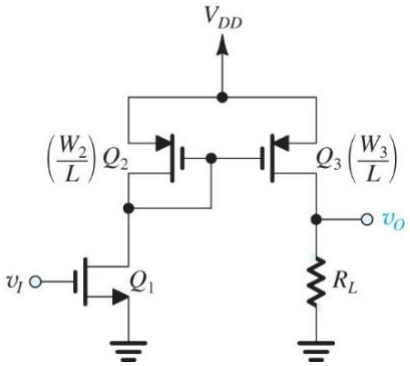
the output voltage will b given by

$$v_o = V_{DD} - V_t + \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}} V_t - \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}} v_I$$

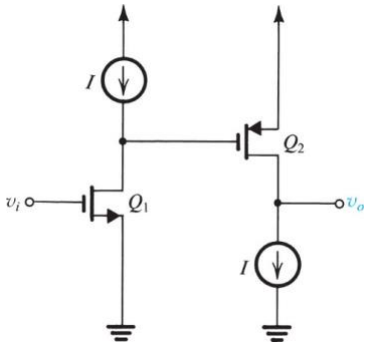
where we have assumed $V_{t1} = V_{t2} = V_t$. Thus the circuit functions as a linear amplifier, even for large input signals. For $(W/L)_1$ = (50 um / 0.5 um), and $(W/L)_2$ = (5 um/0.5 um), find the voltage gain.



2) The circuit here is an amplifier using a current mirror Q_2-Q_3. Here Q_1 is a common source amplifier fed with $v_I = V_{GS} + v_i$, where V_{GS} is the gate-to-source bias voltage of Q_1 and v_i is a small signal to be amplified. Find the output voltage v_o and the voltage gain v_o/v_i. Also find the small-signal resistance of the diode-connected transistor Q_2 in terms of g_{m2}, and the total resistance between the drain of Q_1 and ground. What is the voltage gain of the CS amplifier Q_1? Neglect all r_o's.



3) The amplifier here is formed by cascading two common-source stages. Assuming that $V_{tn} = |V_{tp}|$ and that the biasing current sources have output resistance equal to those of Q_1 and Q_2, find an expression for the overall voltage gain in terms o fg_m and r_o of Q_1 and Q_2. If Q_1 and Q_2 are to be operated with equal overdrive voltages, $|V_{OV}|$, fin dthe required value of $|V_{OV}|$ if $\lambda = 0.2V^{-1}$ and the required gain is 400 V/V.



4) In this common-gate amplifier, Q_2 and Q_3 are matched, $k_n'(W/L)_n = k_p'(W/L)_p = 4\ mA/V^2$, and all transistors have $|V_t| = 0.8V$ and $\lambda = 0.05\ V^{-1}$. The v_{sig} is a small signal with no dc component.
   a) Ignore λ, find the dc drain current of Q_1 and the required value of V_{BIAS}.
   b) Find the values of g_m and r_o of all transistors.
   c) Find the value of R_{in}.
   d) Find the value of R_{out}.
   e) Calculate the voltage gain v_o/v_i and v_o/v_{sig}.
   f) How large can v_{sig} be (peak-to-peak) while maintaining saturation mode operation for Q_1 and Q_2?