

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 130 / EE 230A
Fall 2013

Prof. Liu

Homework Assignment #1

Due at the beginning of class on Thursday, 9/3/13

Problem 1: Moore's law

Read Gordon Moore's 1965 paper "Cramming more components onto integrated circuits," published in the magazine Electronics, then look through his 2003 presentation titled "No exponential is forever" delivered at the International Solid State Circuits Conference (ISSCC). (These are in the bSpace site.)

- a) Where did Moore earn his undergraduate degree?
- b) Why did Moore predict that silicon would be the predominant semiconductor material used for integrated circuits?
- c) Referring to the first plot in Moore's paper: Why is there a minimum cost per component (transistor) as a function of the number of components per integrated circuit? How does this minimum cost point change over time, as integrated circuit manufacturing technology advances? What, then, was the primary reason for increasing the number of components (*i.e.* the complexity) per integrated circuit?
- d) At what rate did Moore originally observe the complexity of integrated circuits to be increasing? In 1975 he revised this rate; what has it been since the early 1970s?
- e) In 2003 Moore noted several exponential trends that are a consequence of Moore's Law. List five of these trends.

Problem 2: Basic units and elements used in semiconductor devices

- a) Common units of length used to describe semiconductor device parameters are the centimeter (cm) and micron or micrometer (μm). **You are expected to be able to easily convert distances between these units on the quizzes and final exam.**

Express the following distances in cm:

- i) 1 μm
 - ii) 1 nanometer (nm)
 - iii) 3 nanometers
 - iv) $0.1 \mu\text{m} = 100 \text{ nm}$
 - v) 1 Ångstrom
- b) The common unit of energy used for semiconductor devices is the electron volt (eV), which is the total amount of kinetic energy gained by a free electron when it is accelerated through a potential difference of one Volt. 1 electron volt (eV) = 1.602×10^{-19} J. Note that the magnitude of electric charge carried by a single electron is $q = 1.6 \times 10^{-19}$ Coulombs.

The product of the Boltzmann constant ($k = 8.62 \times 10^{-5}$ eV/K) and the absolute temperature (T) is approximately 26 meV at room temperature (300K). The thermal voltage is defined to be kT/q and is approximately 26 mV at room temperature. **You are expected to be able to perform the following calculations by hand (*i.e.* without a calculator) on the quizzes and final exam**, knowing that:

$$\ln(a^b) = b \cdot \ln(a)$$

$$kT \cdot \ln(10) = 60 \text{ meV}$$

$$(kT/q) \cdot \ln(10) = 60 \text{ mV}$$

Calculate the following quantities:

- i) $kT \cdot \ln(10^{18}/10^{10})$
- ii) $10^{10} \cdot \exp(0.42 \text{ eV}/kT)$
- iii) $(kT/q) \cdot \ln[(10^{18} \times 10^{16})/10^{20}]$

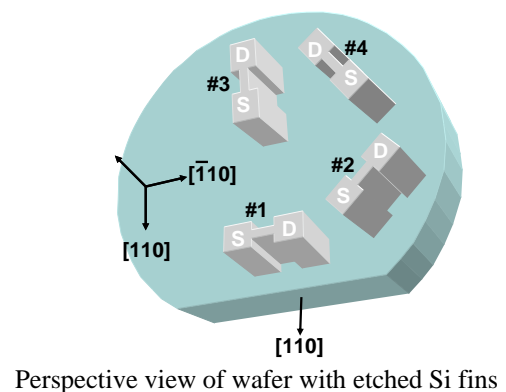
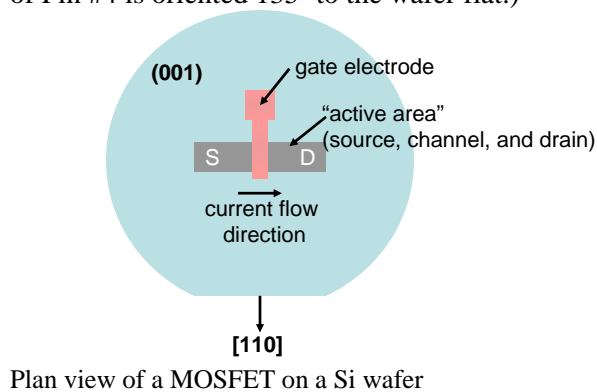
Don't forget to specify units in your answers, where appropriate!

- c) i) What are the two most commonly used p-type dopant species (*i.e.* acceptor atoms) used in silicon?
ii) What are the two most commonly used n-type dopant species (*i.e.* donor atoms) used in silicon?

Problem 3: Miller indices and silicon crystal structure

The performance of a MOSFET depends upon the crystalline orientation of the channel surface as well as the current-flow direction. For an n-channel MOSFET, in which current is carried by electrons, a channel surface with lower atomic density is advantageous for higher performance; whereas for a p-channel MOSFET, in which current is carried by holes, a channel surface with higher atomic density is advantageous for higher performance.

- Given that the lattice constant of Si is 5.43\AA , calculate the areal density of atoms (number/cm²) on each of the following planes: (100), (110), and (111). Based on your answers, which plane would you expect to be best for n-channel MOSFET performance? Which plane would you expect to be best for p-channel MOSFET performance?
- The crystalline orientation of the channel surface is precisely controlled in an integrated-circuit manufacturing process by slicing wafers along (001) planes, and indicating the [110] direction by marking the wafer by a “flat” or notch at the edge of the wafer.
 - If a MOSFET is laid out on the surface of a (001) silicon wafer as shown in the figure below (left), what are the Miller indices for the direction of current flow?
 - The most advanced MOSFET structures today are fabricated along the sidewalls of narrow silicon fins etched into the wafer surface, as shown in the figure below (right). (Current flows along the fin sidewalls between the source (S) and drain (D) regions.) What are the Miller indices for the planes of the fin sidewalls, for each of the 4 fins shown in the figure? (The fin sidewall surface of Fin #1 is parallel to the wafer flat; the fin sidewall surface of Fin #2 is oriented 45° to the wafer flat; the fin sidewall surface of Fin #3 is oriented 90° to the wafer flat, and the fin sidewall surface of Fin #4 is oriented 135° to the wafer flat.)



Problem 4: Intrinsic semiconductor

Refer to the plot of intrinsic carrier concentration (n_i) vs. absolute temperature (T) in the Lecture 1 notes:

- Explain qualitatively the differences in intrinsic carrier concentrations for Ge, Si and GaAs. (Why is n_i highest for Ge? Why is it lowest for GaAs?)
- Explain qualitatively why n_i increases with increasing temperature.
- Integrated-circuit devices rely on extrinsic semiconductor properties (*i.e.* local control of carrier concentrations by doping or by applying an electric field). Which of the semiconductors (Ge, Si and GaAs) would you expect to be best for high-temperature device operation, and why?