UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 130/230A Prof. Liu
Fall 2013

Homework Assignment #10
Due at the beginning of class on Thursday, 11/7/13

Problem 1: MOS Capacitor Non-Idealities

(a) The effect of charge in the gate dielectric of a MOS device is to alter the flat-band voltage:

$$V_{FB} = \phi_{MS} - \frac{Q_F}{C_{ox}} - \frac{1}{\varepsilon_{SiO_2}} \int_0^{x_o} x\rho_{ox}(x)dx - \frac{Q_{IT}(\phi_S)}{C_{ox}}$$

The fixed oxide charge density Q_F (located at the oxide/silicon interface, *i.e.* at $x = x_o$) is typically $\sim 10^{11} q/\text{cm}^2$. If dangling Si bonds at the oxide/silicon interface are "passivated" by hydrogen, then the density of interface traps Q_{IT} is typically below $5\times 10^{10} q/\text{cm}^2$. Ideally, there are no bulk oxide charges, *i.e.* ρ_{ox} is negligible.

Calculate the amount of shift in V_{FB} due to $Q_F \sim 10^{11} q/\text{cm}^2$, for a gate oxide thickness of 5 nm.

How does the impact of oxide charge on V_{FB} change as the gate oxide thickness is reduced?

(b) Explain qualitatively why n^+ poly-Si gate depletion causes the capacitance of an NMOS capacitor to be smaller than the gate-dielectric capacitance $C_{ox}=\varepsilon_{ox}/x_o$ for inversion bias ($V_G > V_T$). How does the gate depletion effect change with increasing gate voltage above V_T?

(c) Explain qualitatively how the thickness of the inversion layer affects the capacitance of an NMOS capacitor. How does the impact of the inversion layer thickness change with increasing gate voltage above V_T?

Problem 2: MOSFET Operation

Consider the basic CMOS inverter circuit (Lecture 19, Slide 8):

(a) What is the role of the NMOS transistor when it is in the on state (when the input voltage is greater than its threshold voltage V_{TN}, *e.g.* when $V_{IN} = V_{DD}$)? In steady state, what is the drain-to-source voltage difference, V_{DS}, when the transistor is ON?

(b) What is the role of the NMOS transistor when it is in the off state (when the input voltage is less than its threshold voltage V_{TN}, *e.g.* when $V_{IN} = 0$ V)? In steady state, what is the drain-to-source voltage difference, V_{DS}, when the transistor is OFF?

(c) Explain why the NMOS and PMOS transistors operate in a complementary manner, when their gate electrodes are electrically connected and their source electrodes are appropriately biased.

Problem 3: The MOSFET as a Resistor

Consider an n^+-poly-Si (4.05 eV work function) gated long-channel n-MOSFET with $W/L = 10$, effective gate-oxide thickness $T_{oxe} = 3$ nm, and substrate (body) dopant concentration $N_A = 5\times 10^{17}\ \text{cm}^{-3}$:

(a) Calculate the gate-to-source voltage V_{GS} required for the MOSFET to present a resistance of 1 kΩ between the source and drain at low values of V_{DS}.
(Note: You will need to solve this problem iteratively when you consider the dependence of effective mobility μ_{eff} on the effective vertical electric field, as shown in Slide 14 of Lecture 19.)

(b) What is the inversion-layer electron density Q_{inv}/q (electrons/cm^2) corresponding to your answer in part (a)?

(c) Using the AC inversion centroid (Slide 16 of Lecture 18) as an estimate of the inversion layer thickness T_{inv}, what is the average carrier concentration (electrons/cm^3) in the inversion layer corresponding to your answer in part (a)?

Problem 4: MOS Threshold Voltage Adjustment

In practice, dopants are implanted into the semiconductor surface of MOS devices in order to fine-tune their threshold voltages during the manufacturing process. The threshold voltage of a MOS transistor also can be dynamically adjusted (after the manufacturing process) by applying a body bias voltage V_B that is different from the source voltage V_S:

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\phi_F + V_{SB})}}{C_{ox}}$$

where $V_{SB} \equiv V_S - V_B$.

Consider an NMOS transistor that is built using n+ poly-Si as the gate material ($\Phi_M = 4.05$ eV) and 3 nm-thick SiO_2 as the gate dielectric on a p-type silicon substrate with $N_A = 10^{17}$ cm^{-3}. (The native threshold voltage of this device is the same as for the MOS device of Homework Assignment #9, Problem 1.)

(a) Suppose you are a process engineer who helps to design the manufacturing process. What implant species (*e.g.* As or B) and dose (#/cm^2) would you specify, to attain a threshold voltage $V_T = 0.2$ V? (Assume that the p-type body is grounded, as is the n+ source of the transistor, so that $V_{SB} = 0$ V.)

(b) Suppose you are a circuit designer who is stuck with an NMOS transistor that is manufactured with n+ poly-Si gate material ($\Phi_M = 4.05$ eV) and 3 nm-thick SiO_2 gate dielectric on a p-type silicon substrate with $N_A = 10^{17}$ cm^{-3}. How would you bias the body of the transistor to tune the threshold voltage V_T to be 0.2 V?